RTM875N-397 AC Performance Measurement Report

Measurement Equipment :

Clock Rise Time / Fall Time Are Measured by Tektronix® 6804B with Single-ended Probe

- Mainframe with 8.0GHz Bandwidth
- Mainframe with 20GS/s Sampling Rate
- P7240 Active Probe with 4.0GHz Bandwidth (input: 1.0pF / 20K-ohm)

Clock Jitter & Duty Cycle Are Measured by Tektronix® 6804B with Differential Probe

- P7330 Differential Active Probe with 3.5GHz Bandwidth (input: 0.5pF / 100K-ohm)
- Tektronix® Jitter Analysis 3® Jitter Measurement Software

Measurement Environment :

- Test board

Measurement Item :

Differential Clock

- Slew_Rise & Slew_Fall
- Vcross & ΔVcross
- Cycle to Cycle jitter
- Vmax & Vmin
- Duty Cycle

Single-end Clock

- Slew_Rise & Slew_Fall
- Duty Cycle
- Cycle to Cycle jitter
-

Measurement Summary

From the measurement shown as follows, RTM875N-397 works good and meets all CLK Spec.

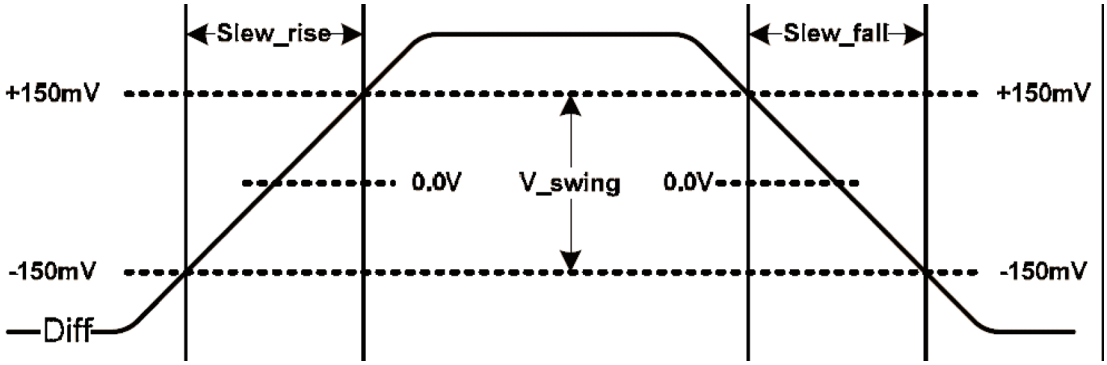
Measurement Signal:

1.**CPU0 CLOCK**	2. **CPU1 CLOCK**	3.**SATA CLOCK**
4.**PCIE6 CLOCK**	5.**PCIE11 CLOCK**	6. **DOT96 CLOCK**
7.**PCI CLOCK**	8.**USB CLOCK**	9. **REF CLOCK**
10.**Phase jitter**		

Measurement Condition

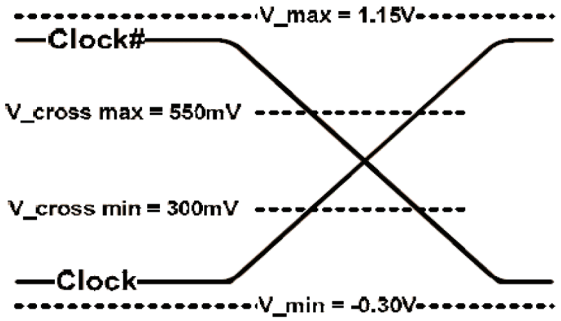
#1 Slew_Rise & Slew_Fall Of Differential Waveform :

Rise and fall slew rate are measured differential waveform between +150mV and -150mV on the rising and falling edges of the clock.
(Reference CK505 spec page.19 / 20)



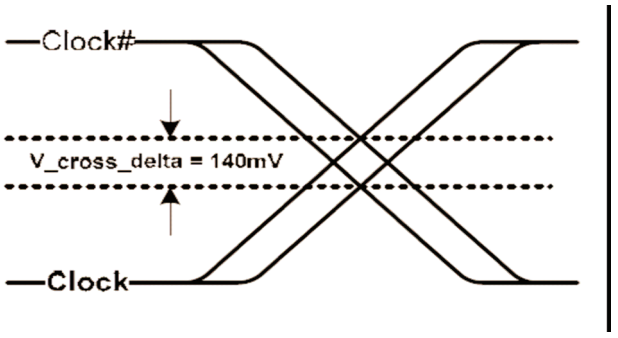
#2 Vcross Of Differential Waveform :

Absolute cross point= 0.3 ~0.55 V (Reference CK505 spec page.19 / 20)



#3 ΔVcross Of Differential Waveform :

Absolute ΔVcross <140 mV (Reference CK505 spec page.19 / 20)

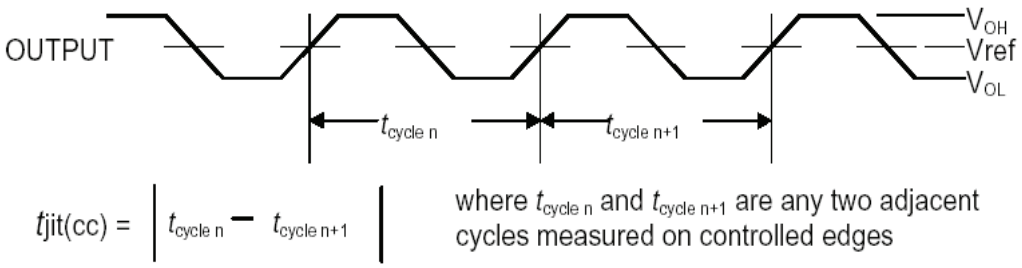


#4 Cycle to Cycle jitter :

Absolute Cycle to Cycle jitter <85 ps

(Reference CK505 spec page.19 / 20 & JEDEC JESD65-A page.13)

cycle-to-cycle period jitter (*t*jit(cc)): The variation in cycle time of a signal between adjacent cycles, over a random (i.e., not synchronous to the signal) sample of adjacent cycle pairs.



An example of an output waveform and cycle-to-cycle period jitter measurement.

#5 Vmax & Vmin :

Vmax < 1.15 V and Vhigh > -0.3V.

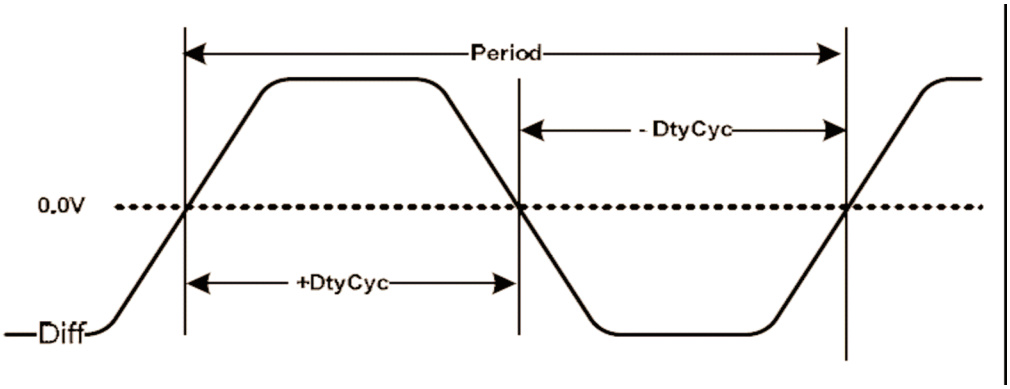
Measure the Vmax & Vmin value by using Tektronix Scope “Vmax ” & “Vmin” function.

(Reference CK505 page.18)

#6 Duty Cycle :

Duty cycle specification is between 45 and 55%.

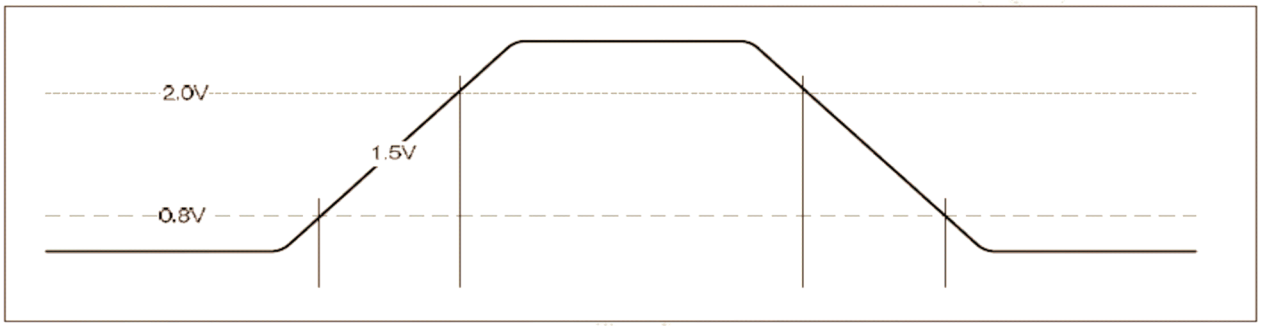
(Reference CK505 page.19)



#7 Slew_Rise & Slew_Fall Of Single Waveform:

Rise and fall slew rate are measured single waveform between 0.8V and 2.0V on the rising and falling edges of the clock.

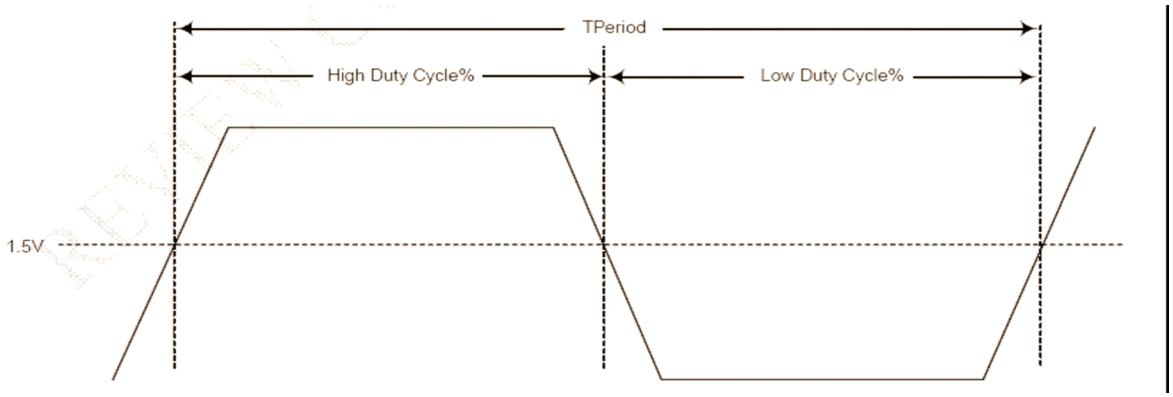
(Reference CK505 spec page.20~22)



#8 Duty Cycle Of Single Waveform :

Duty cycle specification is between 45 and 55%.

(Reference CK505 page.20~23)



#4 Cycle to Cycle jitter :

(Reference CK505 spec page.20~23 & JEDEC JESD65-A page.13)

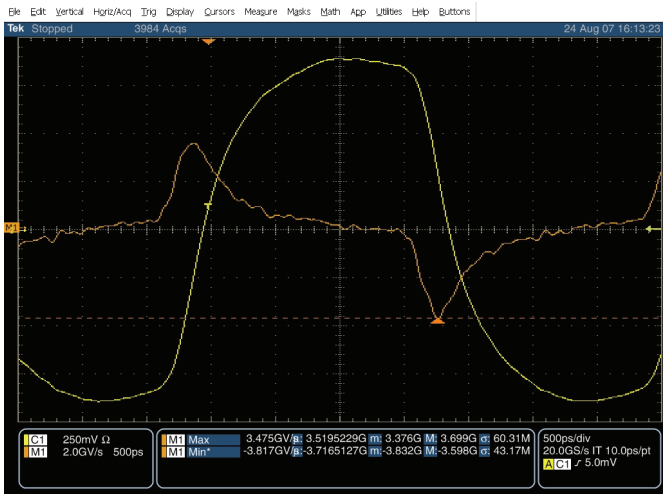
Parameter	Description	Max	Units	Signal	Note
CPU_Jit_cc	Jitter mag (cycle to cycle)	85	ps	Diff	1
SRC_Jit_cc	Jitter mag (cycle to cycle)	125	ps	Diff	1
DOT_Jit_cc	Jitter mag (cycle to cycle)	250	ps	Diff	1
USB_Jit_cc	Jitter mag (cycle to cycle)	350	ps	SE	
PCI_Jit_cc	Jitter mag (cycle to cycle)	500	ps	SE	
REF_Jit_cc	Jitter mag (cycle to cycle)	1000	ps	SE	

Note

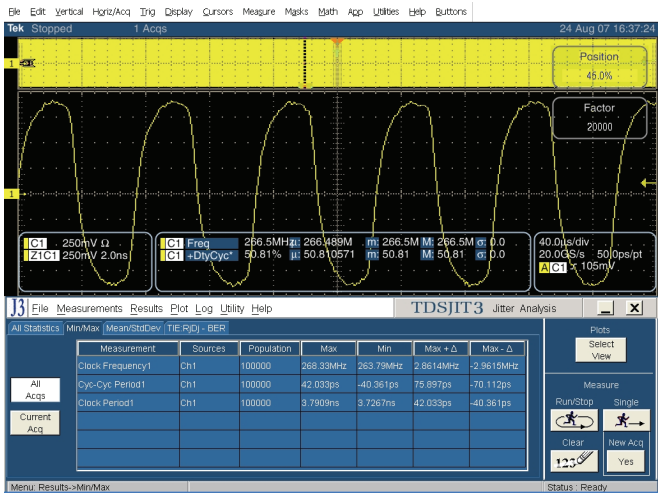
1. Jitter specifications are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers as the in system performance will be degraded somewhat. The receiver EMTS (Chipset or CPU) will have the receiver jitter specifications as measured in a real system.

1. CPU0 CLOCK

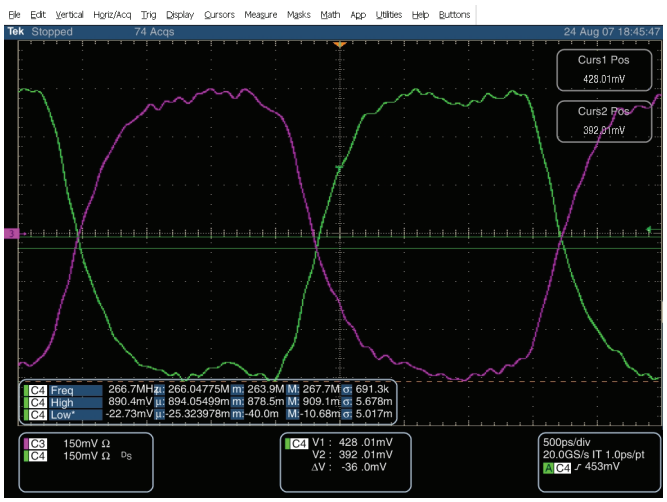
	Slew_Rise	Slew_Fall	Vcross	ΔV_{CROSS}	C-C jitter
Specification	2.5~8 V/ns See #1	2.5~8 V/ns See #1	300~550 mV See #3	ΔV_{CROSS} <140 mV See #3	< 85 ps See #2
Measured Result	**3.519 V/ns**	**3.716 V/ns**	**392 ~ 428 mV**	**36 mV**	**42 ps**
	Vmax	Vmin	Duty Cycle		
Specification	< 1.15V See #4	> -0.3V See #4	45%~55% See #2		
Measured Result	**0.890 V**	**-0.023 V**	**50.81 %**		



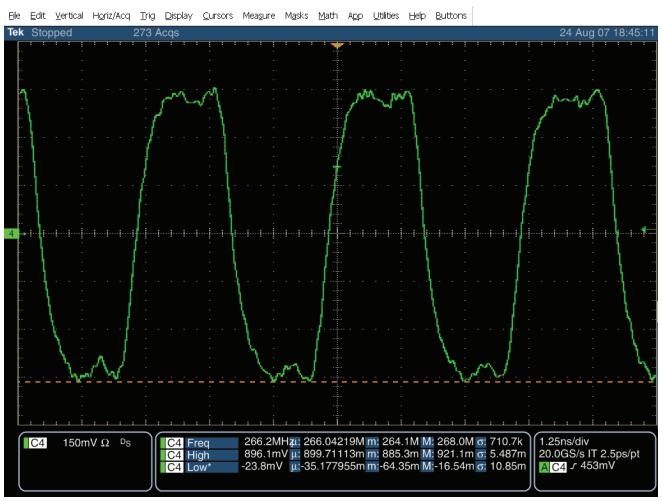
Slew_Rise & Slew_Fall



Cycle to Cycle jitter & Duty Cycle



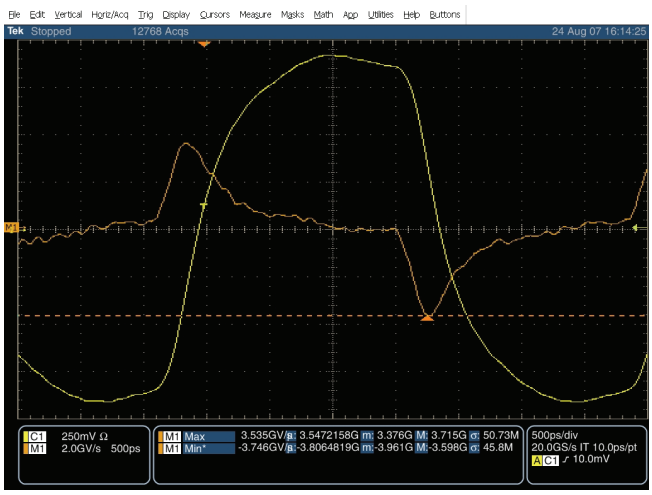
Vcross & ΔVcross



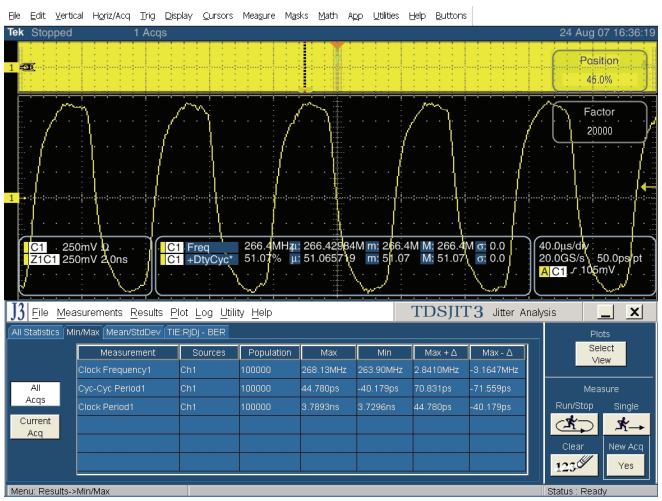
Vmax & Vmin

2. CPU1 CLOCK

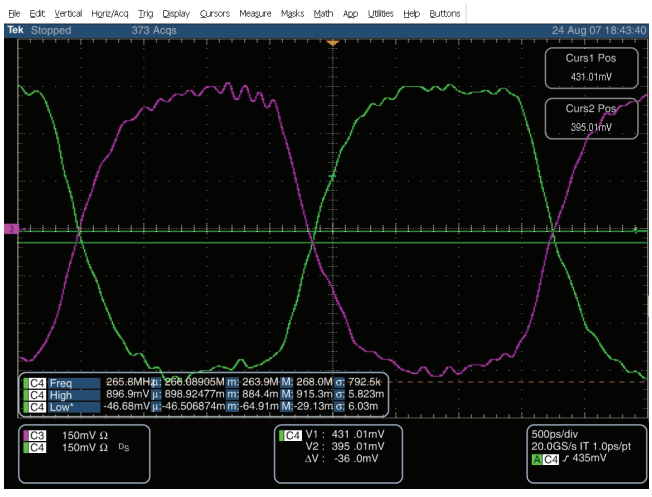
	Slew_Rise	Slew_Fall	Vcross	ΔV_{CROSS}	C-C jitter
Specification	2.5~8 V/ns See #1	2.5~8 V/ns See #1	300~550 mV See #3	ΔV_{CROSS} <140 mV See #3	< 85 ps See #2
Measured Result	**3.535 V/ns**	**3.746 V/ns**	**395 ~ 431 mV**	**36 mV**	**44 ps**
	Vmax	Vmin	Duty Cycle		
Specification	< 1.15V See #4	> -0.3V See #4	45%~55% See #2		
Measured Result	**0.897 V**	**-0.047 V**	**51.07 %**		



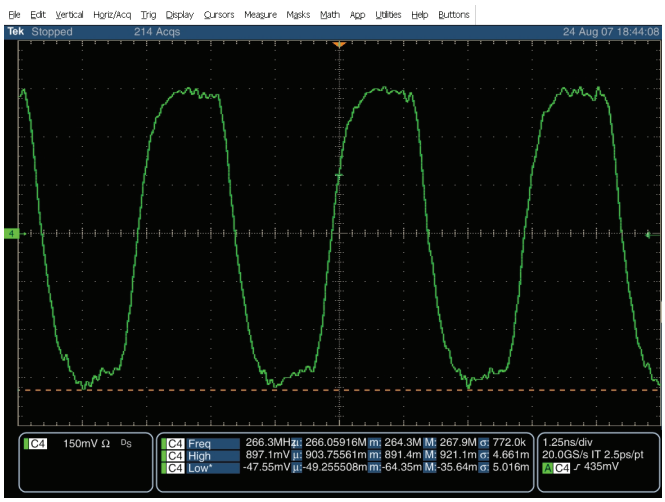
Slew_Rise & Slew_Fall



Cycle to Cycle jitter & Duty Cycle



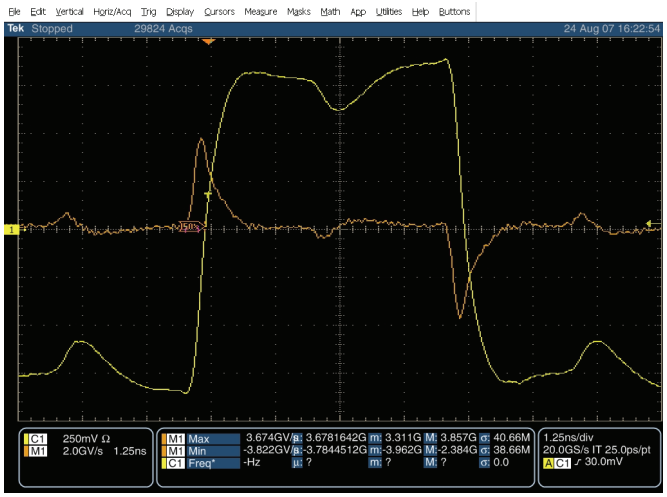
Vcross & ΔVcross



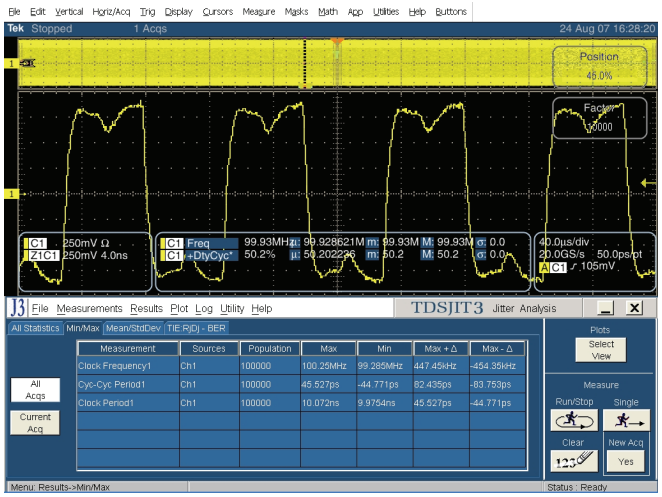
Vmax & Vmin

3. SATA CLOCK

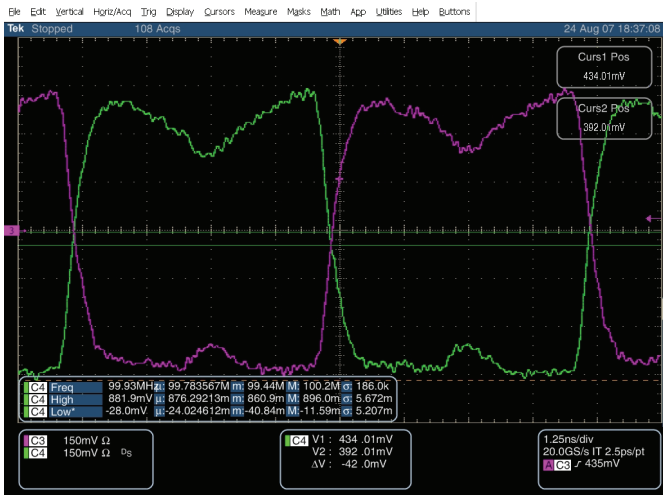
	Slew_Rise	Slew_Fall	Vcross	ΔV_{CROSS}	C-C jitter
Specification	2.5~8 V/ns See #1	2.5~8 V/ns See #1	300~550 mV See #3	ΔV_{CROSS} <140 mV See #3	< 125 ps See #2
Measured Result	**3.674 V/ns**	**3.822 V/ns**	**392~ 434 mV**	**42mV**	**45 ps**
	Vmax	Vmin	Duty Cycle		
Specification	< 1.15V See #4	> -0.3V See #4	45%~55% See #2		
Measured Result	**0.884**	**-.023V**	**50.2**		



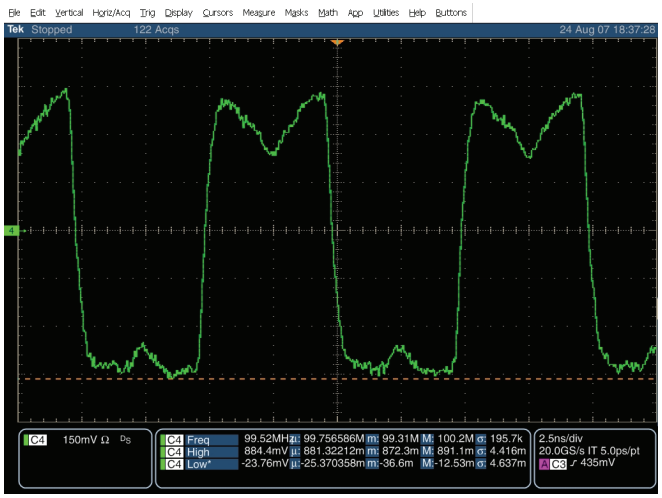
Slew_Rise & Slew_Fall



Cycle to Cycle jitter & Duty Cycle



Vcross & ΔVcross

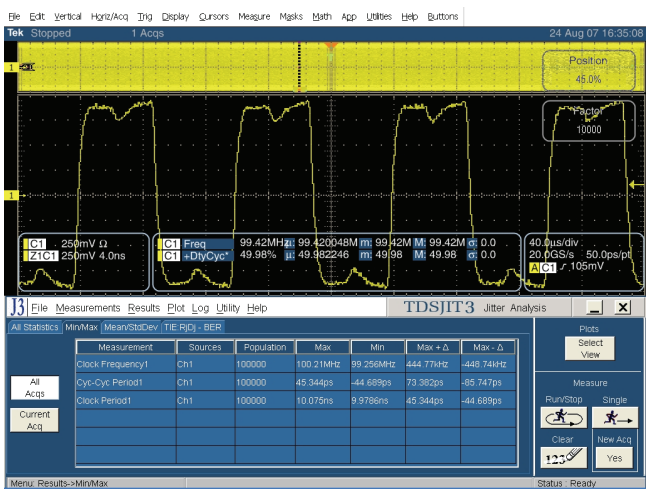


Vmax & Vmin

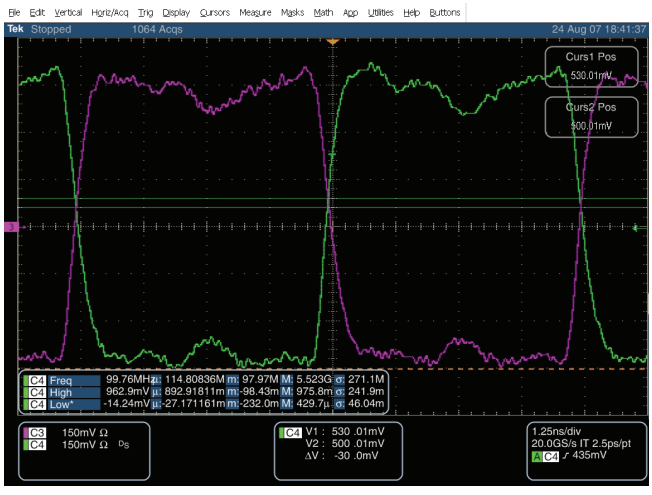
4. PCIE6 CLOCK

	Slew_Rise	Slew_Fall	Vcross	ΔV_{CROSS}	C-C jitter
Specification	2.5~8 V/ns See #1	2.5~8 V/ns See #1	300~550 mV See #3	ΔV_{CROSS} <140 mV See #3	< 125 ps See #2
Measured Result	**3.939 V/ns**	**3.935 V/ns**	**500 ~ 530 mV**	**30 mV**	**45 ps**
	Vmax	Vmin	Duty Cycle		
Specification	< 1.15V See #4	> -0.3V See #4	45%~55% See #2		
Measured Result	**0.962 V**	**-0.014 V**	**49.98 %**		

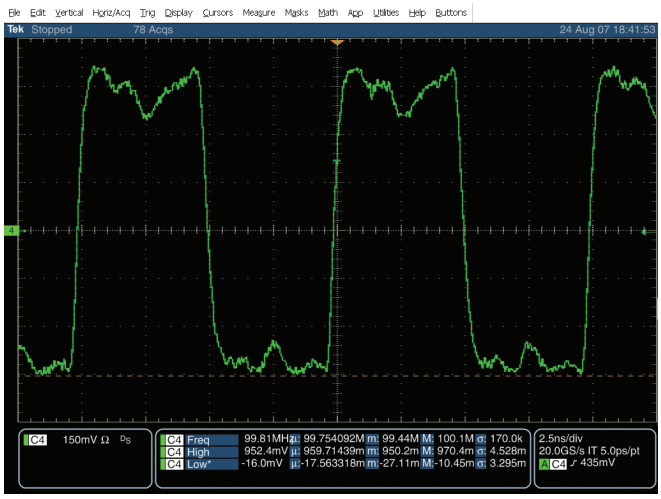
Slew_Rise & Slew_Fall



Cycle to Cycle jitter & Duty Cycle



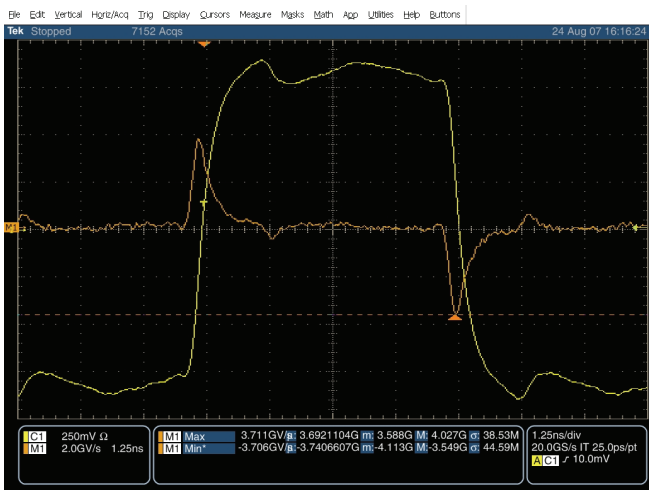
Vcross & ΔVcross



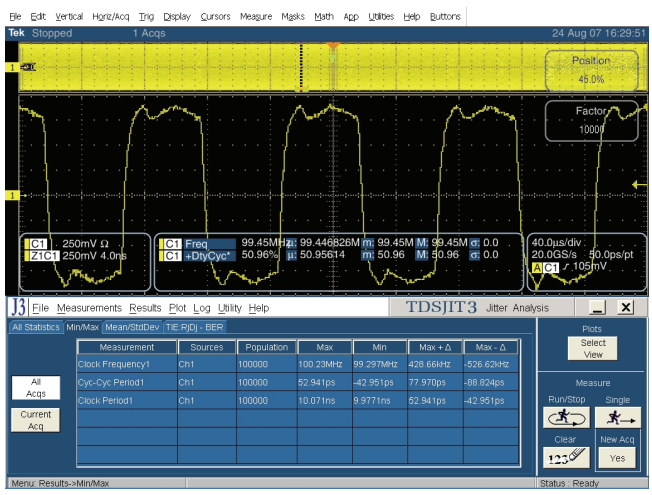
Vmax & Vmin

5. PCIE11 CLOCK

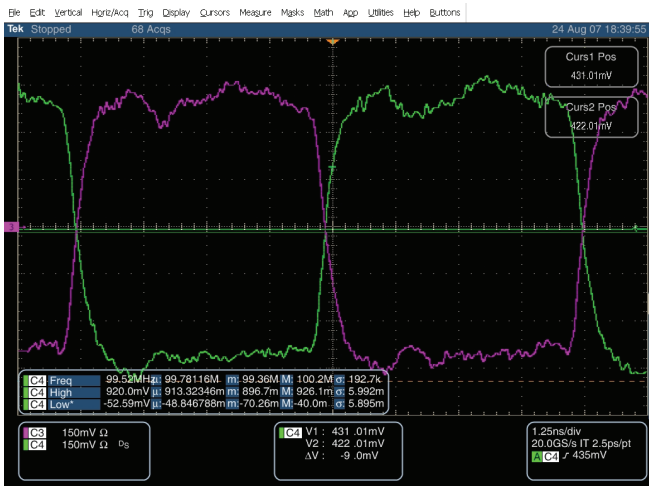
	Slew_Rise	Slew_Fall	Vcross	ΔV_{CROSS}	C-C jitter
Specification	2.5~8 V/ns See #1	2.5~8 V/ns See #1	300~550 mV See #3	ΔV_{CROSS} <140 mV See #3	< 125 ps See #2
Measured Result	**3.711 V/ns**	**3.706 V/ns**	**422 ~ 431 mV**	**9 mV**	**52 ps**
	Vmax	Vmin	Duty Cycle		
Specification	< 1.15V See #4	> -0.3V See #4	45%~55% See #2		
Measured Result	**0.920 V**	**- 0.052 V**	**50.96 %**		



Slew_Rise & Slew_Fall



Cycle to Cycle jitter & Duty Cycle

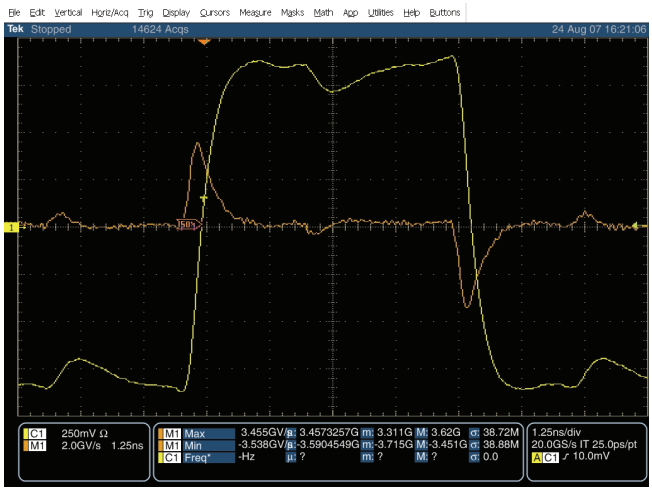


Vcross & ΔVcross

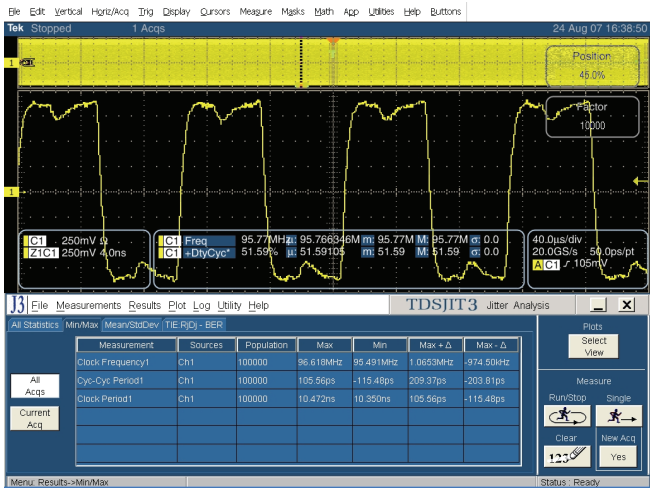
Vmax & Vmin

6. DOT96 CLOCK

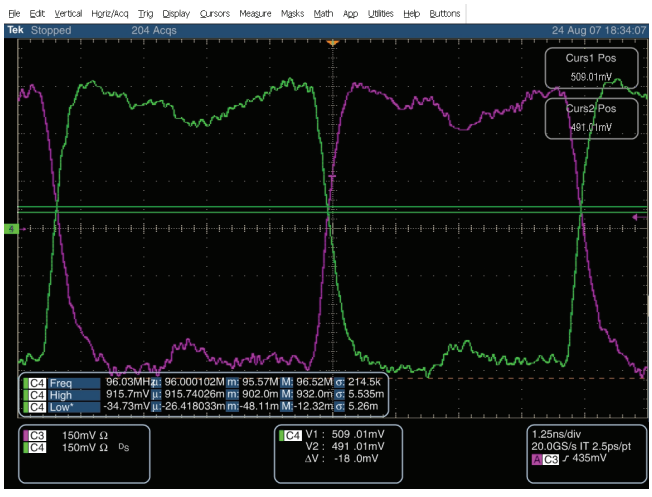
	Slew_Rise	Slew_Fall	Vcross	ΔV_{CROSS}	C-C jitter
Specification	2.5~8 V/ns See #1	2.5~8 V/ns See #1	300~550 mV See #3	ΔV_{CROSS} <140 mV See #3	< 250 ps See #2
Measured Result	**3.455 V/ns**	**3.538 V/ns**	**491 ~ 509 mV**	**51.96 mV**	**115 ps**
	Vmax	Vmin	Duty Cycle		
Specification	< 1.15V See #4	> -0.3V See #4	45%~55% See #2		
Measured Result	**0.914 V**	**- 0.028 V**	**51.59 %**		



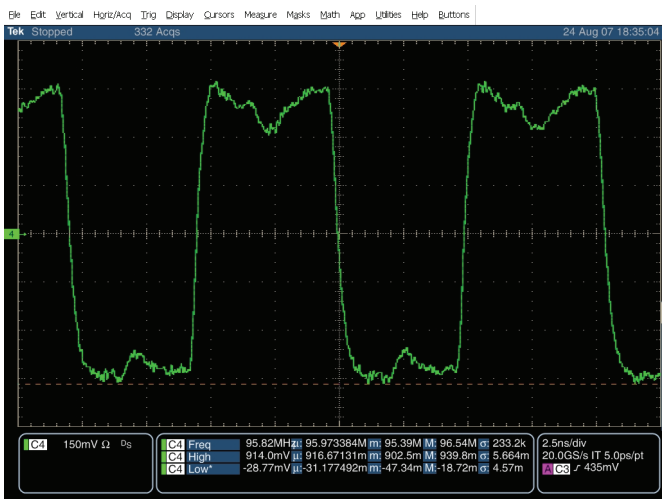
Slew_Rise & Slew_Fall



Cycle to Cycle jitter & Duty Cycle



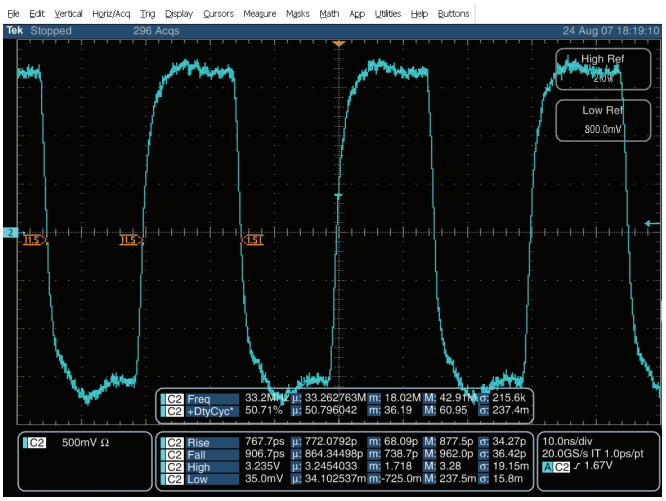
Vcross & ΔVcross



Vmax & Vmin

7.PCI1 CLOCK

	Slew_Rise	Slew_Fall	Duty Cycle	C-C jitter
Specification	1~4 V/ns See #1	1~4 V/ns See #1	45%~55%	< 500 ps See #2
Measured Result	**1.56 V/ns**	**1.32 V/ns**	**50.81 %**	**196 ps**

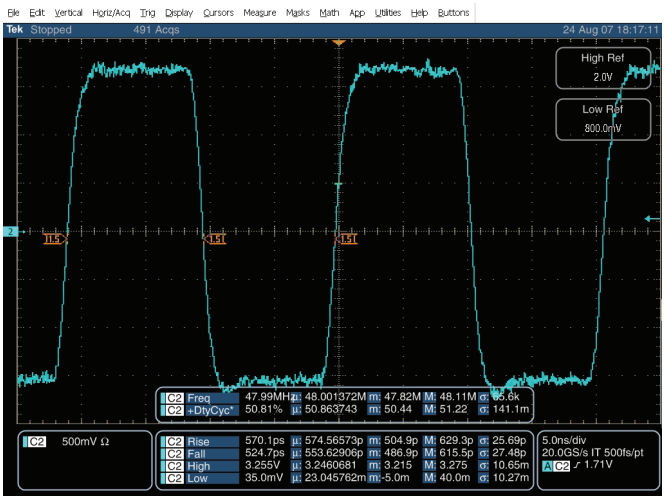


Slew_Rise & Slew_Fall

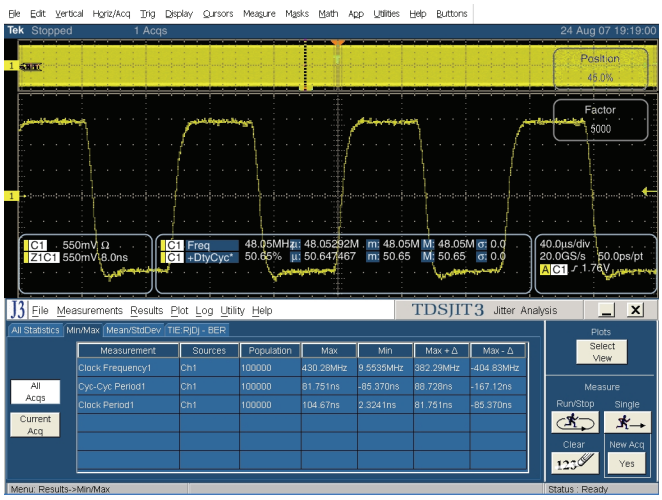
Cycle to Cycle jitter & Duty Cycle

8.USB CLOCK

	Slew_Rise	Slew_Fall	Duty Cycle	C-C jitter
Specification	1~2 V/ns See #1	1~2 V/ns See #1	45%~55%	< 350 ps See #2
Measured Result	**2.01 V/ns**	**2.29 V/ns**	**50.65 %**	**85 ps**



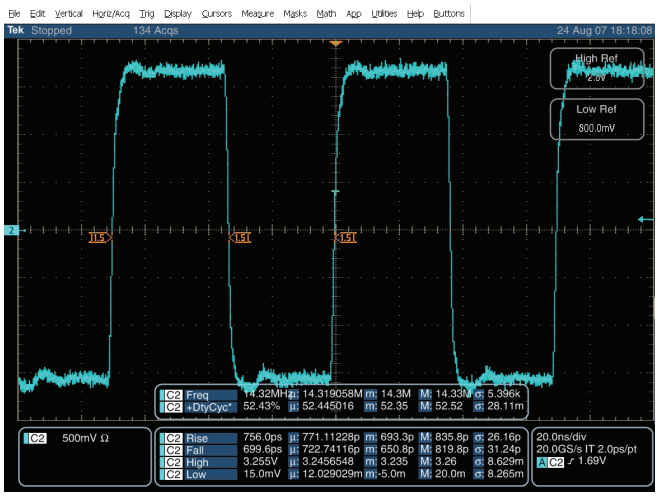
Slew_Rise & Slew_Fall



Cycle to Cycle jitter & Duty Cycle

9. REF1 CLOCK

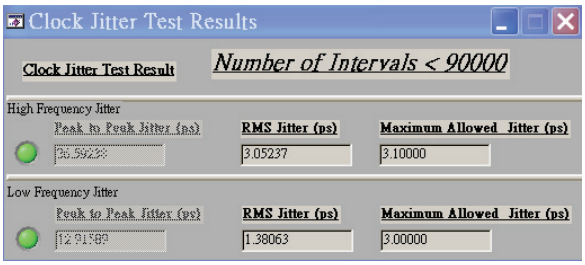
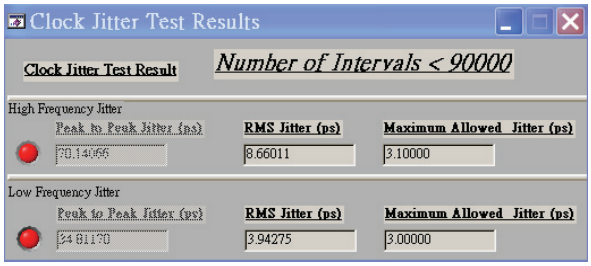
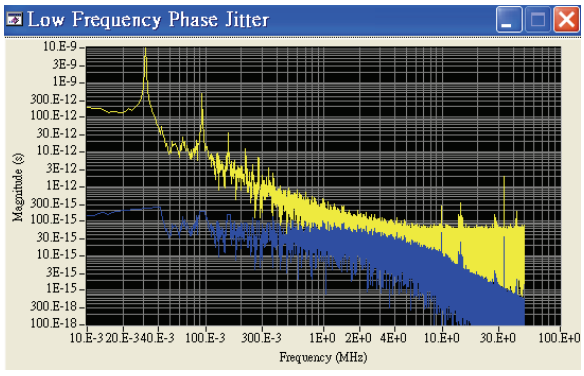
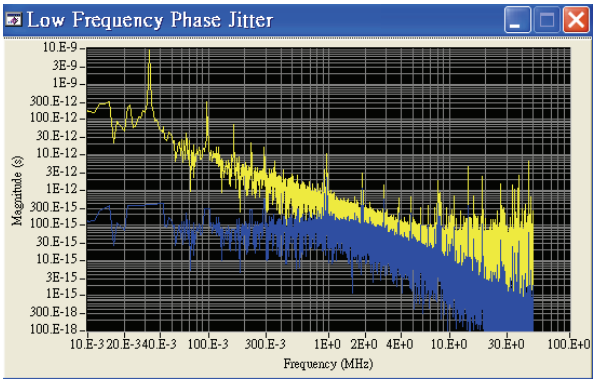
	Slew_Rise	Slew_Fall	Duty Cycle	C-C jitter
Specification	1~4 V/ns See #1	1~4 V/ns See #1	45%~55%	< 1000 ps See #2
Measured Result	**1.59 V/ns**	**1.72 V/ns**	**52.45 %**	**198 ps**

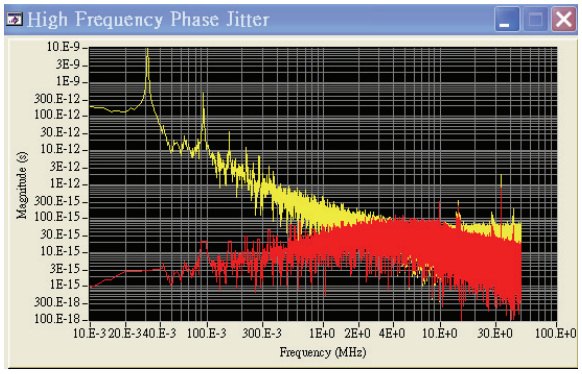


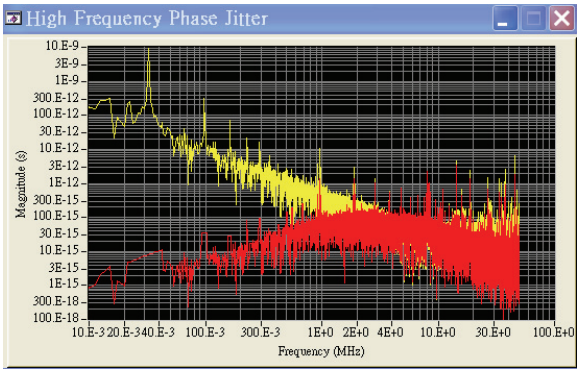
Slew_Rise & Slew_Fall

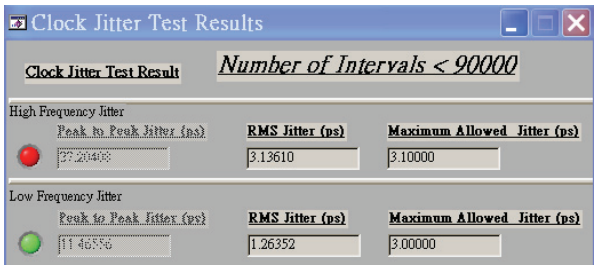
Cycle to Cycle jitter & Duty Cycle

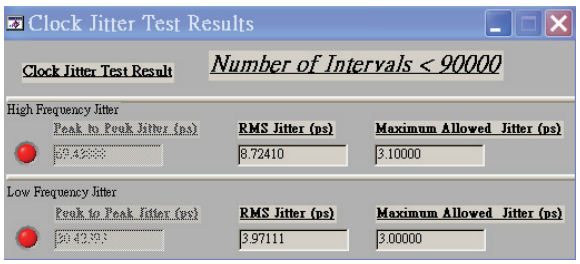
10. Phase jitter

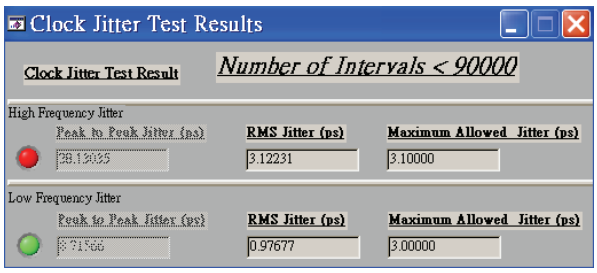
RTM875N-397	IXX-397
	
	

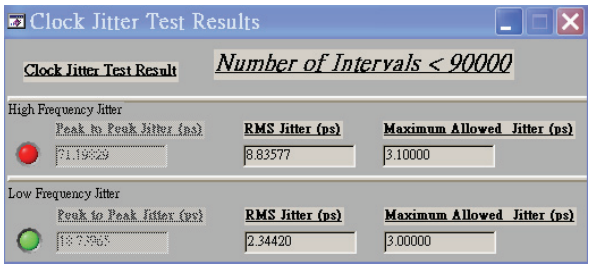


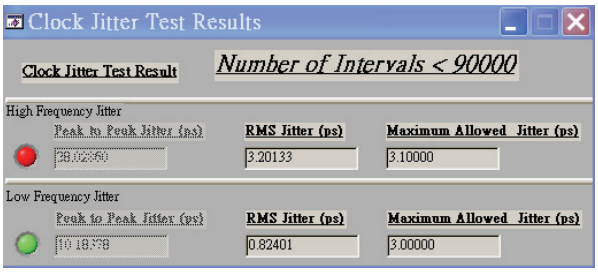


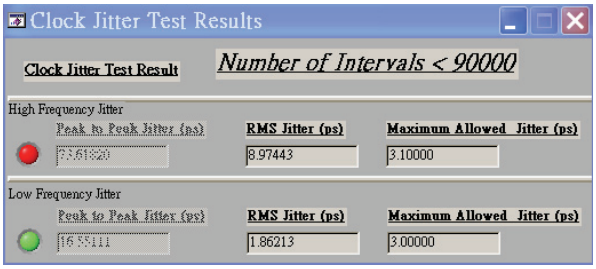












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