88E6390/88E6190/88E6290 Datasheet

11-Port GE AVB/TSN Switch with 8 integrated PHYs and 2 SERDES

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Preface

About this Document

The 88E6390/88E6190/88E6290 datasheet is part of a multi-part set that includes the following documents:

- **Link Street® 88E6390X/88E6390/88E6290/88E6190X/88E6190/88E6190R Switch Functional Specification**
  Provides a functional description of the device core.

- **Link Street® 88E6390X/88E6390/88E6290/88E6190X/88E6190/88E6190R PHY and SERDES Functional Specification**
  Provides a functional description of the PHY and SERDES.

- **Link Street® Integrated Micro Processor (IMP) Functional Specification**

Provides a description of the Integrated Micro Processor.

88E6390/88E6190/88E6290 Datasheet

11-Port GE AVB/TSN Switch with 8 integrated PHYs and 2 SERDES

OVERVIEW

The Marvell® 88E6390/88E6190/88E6290 device is a single-chip integration of a 11-port Ethernet switch with eight integrated Gigabit Ethernet transceivers and two SerDes interfaces. The device contains eight 10/100/1000 triple speed Ethernet transceivers (PHYs), two SerDes interfaces and one digital interface that supports a combination of RGMII, MII, and RMII interfaces in a 144-lead QFP package.

The tenth and eleventh ports provide two Serdes interfaces supporting 2500BASE-X (2.5Gbps) 1000BASE-X, and SGMII.

The device has a high-speed, non-blocking eight traffic class QoS switch fabric that uses the unique Marvell Dynamic Queue Limit architecture. The QoS architecture switches packets into one of eight traffic class queues based upon Port, IEEE 802.1p, IPv4 Type of Service (TOS) or Differentiated Services (Diff-Serv), IPv6 Traffic Class, 802.1Q VLAN ID, DA MAC address or SA MAC address. The device also contains a high-performance address lookup engine with support for up to 16K active nodes, and a 2 Mbit frame buffer memory.
Back-pressure and pause frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion. The MAC units in the devices comply fully with the applicable sections of IEEE 802.3 and support frame sizes up to 10KBytes.

The 88E6390 device includes a TCAM-based Policy Control List (PCL) engine that supports 256 rules. The PCL engine can inspect the first 48 bytes of a frame with a full48 byte match. Rules can be combined to inspect the first 96 bytes of a frame with a full 96 byte match. Actions supported include rule based filtering, VLAN assignment, QoS remarking, and policy based switching.The device's RGMII (or MII/RMII) interface supports a direct connection to Management or Router CPUs with integrated MACs. This interface, along with BPDU handling for IEEE 802.1D Spanning Tree Protocol, 802.1w Rapid Spanning Tree, 802.1s Multiple VLAN Spanning Tree, programmable per-port VLAN configurations, 802.1Q and Port States, supports fully managed switches and truly isolated WAN vs. LAN firewall applications. The device supports 4,096 802.1Q VLAN IDs which can be enabled on a per port basis. Three levels of 802.1Q security is supported with error frame trapping and logging.

The PHY units in the device support the latest 802.3az Energy Efficient Ethernet (EEE) standard. They are designed with Marvell® cutting-edge mixed-signal processing technology for digital implementation of adaptive equalization and clock data recovery. The device also integrates MDI interface termination resistors into the PHYs. This resistor integration facilitates board layout and reduces board cost by reducing the number of external components. Both the PHY and MAC units in the devices comply fully with the applicable sections of IEEE 802.3, IEEE 802.3u, and IEEE 802.3x standards.

The PHYs also include an integrated Advanced Virtual Cable Tester® (VCT™) enabling fault detection and advanced cable performance monitoring.

The 88E6390 also includes an integrated 200MHz microprocessor with 60Kbytes of integrated RAM. The microprocessor's has direct access to all switch registers and its integrated Ethernet controller enables support for Ethernet protocols as well as lightly managed or smart switches.

The device's many operating modes can be configured using SMI (serial management interface - MDC/MDIO) or through the Remote Management Interface. The device also supports a standalone QoS mode or configuration via a low cost serial EEPROM.

Highlighted Features

- Integrated 200MHz Z80 compatible microprocessor
  - Integrated60Kbyte zero wait state RAM
  - Boots via EEPROM, SMI interface, or Remote Management Unit
  - Integrated Ethernet NIC connects directly to switch fabric
- Supports 802.1 AVB/TSN Standards
  - 802.1AS - Precise Timing Protocol
  - 802.1Qat - Stream Reservation Protocol
  - 802.1Qav - Egress Pacing and Shaping
  - 802.1Qbv - Time Aware Shaping
- Supports 1588v2 over Layer 2 and Layer 4
- Timing Application Interface for AVB/TSN end nodes
- Supports Synchronous Ethernet
- Supports Cut-through switch fabric for low latency applications
- TCAM-based Policy Control List (PCL) Engine
  - Line rate, ingress packet classification and filtering based on packet's first 48 or 96 bytes
  - 256 rules of 48 bytes or 128 rules of 96 bytes with independent bit-by-bit masking capability per rule
  - Allows co-existence of short (48B) and long (96B) rules
  - Flexible actions including filtering, VLAN assignment, QoS remarking, and policy based switching
  - Rules can be assigned to any combination of ingress or egress ports
- Supports 802.3az Energy Efficient Ethernet
- Wire speed performance with Maximum Frame size up to 10K Bytes
- 'Best-in-Class' per port TCP/IP Ingress Rate Limiting along with independent Storm Prevention
  - 5 Ingress Rate Limiting buckets per port, supporting Rate-based and Priority-based rate limiting
  - Non-Rate Limited frames based on SA or DA
- Supports 802.1Qbb Priority Based Flow Control

Features

- Quality of Service support with 8 traffic classes
- QoS determined by Port, IEEE 802.1p tagged frames, IPv4's Type of Service (TOS) & Differentiated Services (DS), IPv6's Traffic Class 802.1Q VID, Destination MAC address, or Source MAC address
- Frame and Queue priority overrides based on DA, SA, VID, Ethertype, BC, IP, PPPoE, ARP, or Snoop
- Strict, Weighted, or mixed mode QoS selectable per port
- Programmable QoS weighting via a 128-entry table
- Wake-on-LAN and Wake of Frame Event Detection
- Remote Management capabilities allow device configuration and readback via Ethernet frames
- Supports 16K MAC addresses and 4K VLAN IDs
- Enhanced 802.1s Per VLAN Spanning Tree supporting up to 64 spanning tree instances
- Per port, programmable MAC hardware address learn limiting
- 2 integrated SerDes interfaces
  - Supports 2500BASE-X, 1000BASE-X, and SGMII
- 8 integrated Gigabit Ethernet PHYs fully compliant with the applicable sections of IEEE802.3 and IEEE802.3u
  - Integrated MDI interface termination resistors
  - Integrated Advanced Virtual Cable Tester® (VCT™) cable diagnostic feature
- RGMII/MII/RMII interface supporting 1.8V, 2.5V, or 3.3V I/O
- Supports 2-Wire EEPROMs for configuration
  - 32Kbit to 512Kbit densities supported
  - Able to program attached EEPROMs to save configurations
- 16 x 16mm 144-lead QFP package

Applications

- Gigabit Ethernet switch with 8 1000BASE-TX LAN ports with 2.5Gbps uplinks

Table 1 shows the 88E6390/88E6190/88E6290 device feature differences.

Table 1: 88E6390/88E6190/88E6290 Device Differences

		88E6390	88E6190	88E6290
Features	# GE PHYs	8	8	0
	# FE PHYs	0	0	8
	# RGMII/MII/RMII	1	1	1
	# SerDes with 1 Gbps	2	2	2
	# SerDes with 2.5 Gbps	2	2	2
	XAUI/RXAUI	0	0	0
	Packet Buffer Memory	2 Mbit	2 Mbit	2 Mbit
	Jumbo Frame Support	10K Bytes	10K Bytes	10K Bytes
	# MAC Addresses	16K	16K	16K
QoS	Queues per Port	8	8	8
	802.1p, Port, TOS/DS, IPv6 TC, MAC	Yes	Yes	Yes
	Programmable Weighting	Yes	Yes	Yes
VLAN	Port-based VLANs	Yes	Yes	Yes
	802.1Q VLANs	4096	4096	4096
	Double Tagging (Q in Q)	Yes	Yes	Yes
Mgmt	Wake On LAN / Wake On Frame	Yes	Yes	Yes
	Remote Mgmt/Ethertype DSA	Yes	Yes	Yes
	Layer 2 PCLs	Yes	Yes	Yes
	TCAM	Yes	No	Yes
	802.1D/s/w Spanning Tree	Yes	Yes	Yes
	802.1X Port & MAC Authentication	Yes	Yes	Yes
	Port Mirroring/Port Trunking	Yes	Yes	Yes
	IGMP/MLD Snooping	Yes	Yes	Yes
AVB	802.1AS / Qat / Qav / 1588	Yes	No	Yes
	802.1Qbv	Yes	No	Yes
	1 Step PTP	Yes	No	Yes
	Timing App I/F (TAI)	Yes	No	Yes
Other	Integrated Micro Processor	Yes	Yes	Yes
	Synchronous Ethernet	Yes	No	Yes
	Cut Through Switch Fabric	Yes	No	Yes
	Ingress Rate Limiting Resources	5/port	5/port	5/port
	GPIO Pins (shared)	16	16	16

Figure 1: 88E6390 Block Diagram

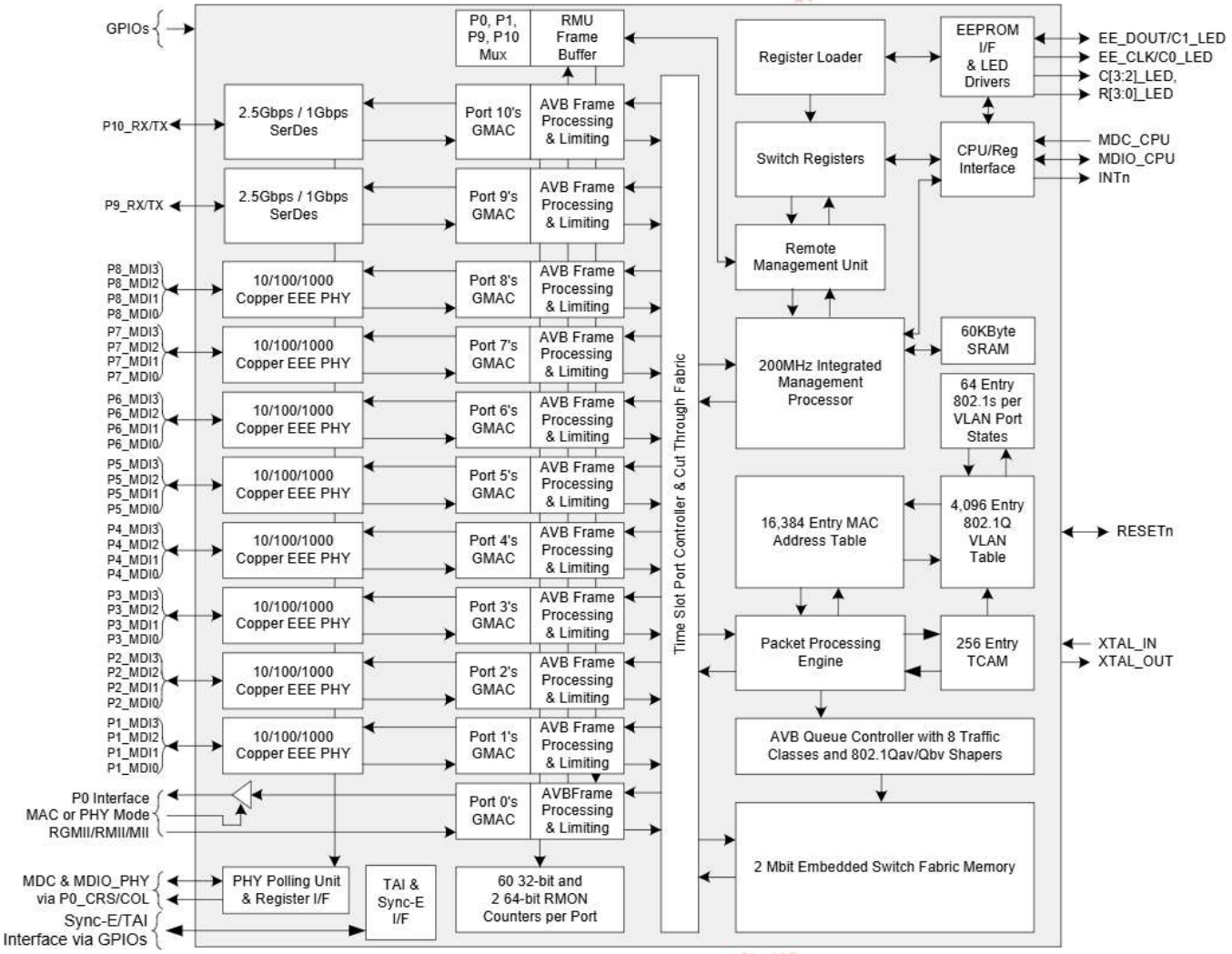


Figure 2: 88E6190 Block Diagram

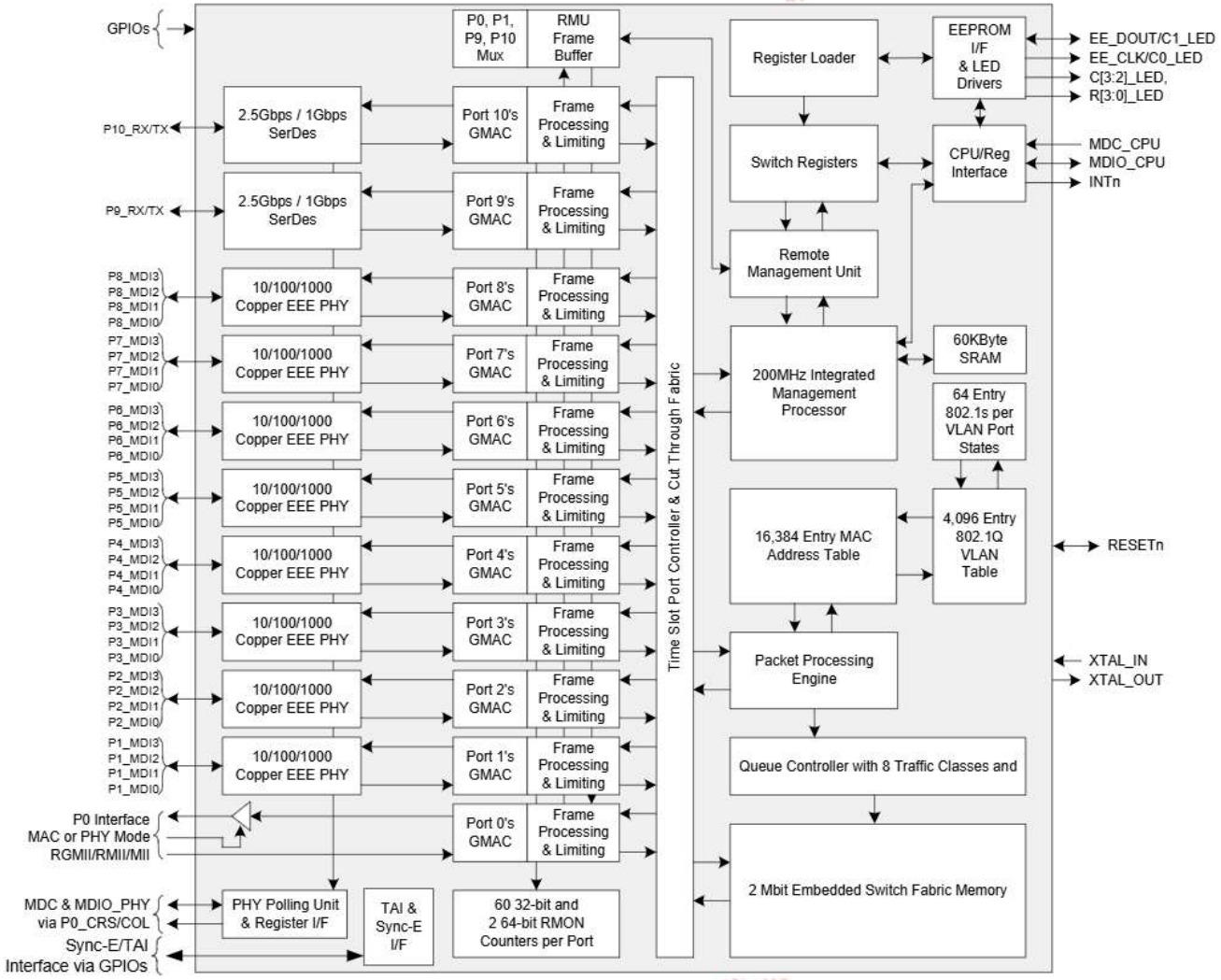


Figure 3: 88E6290 Block Diagram

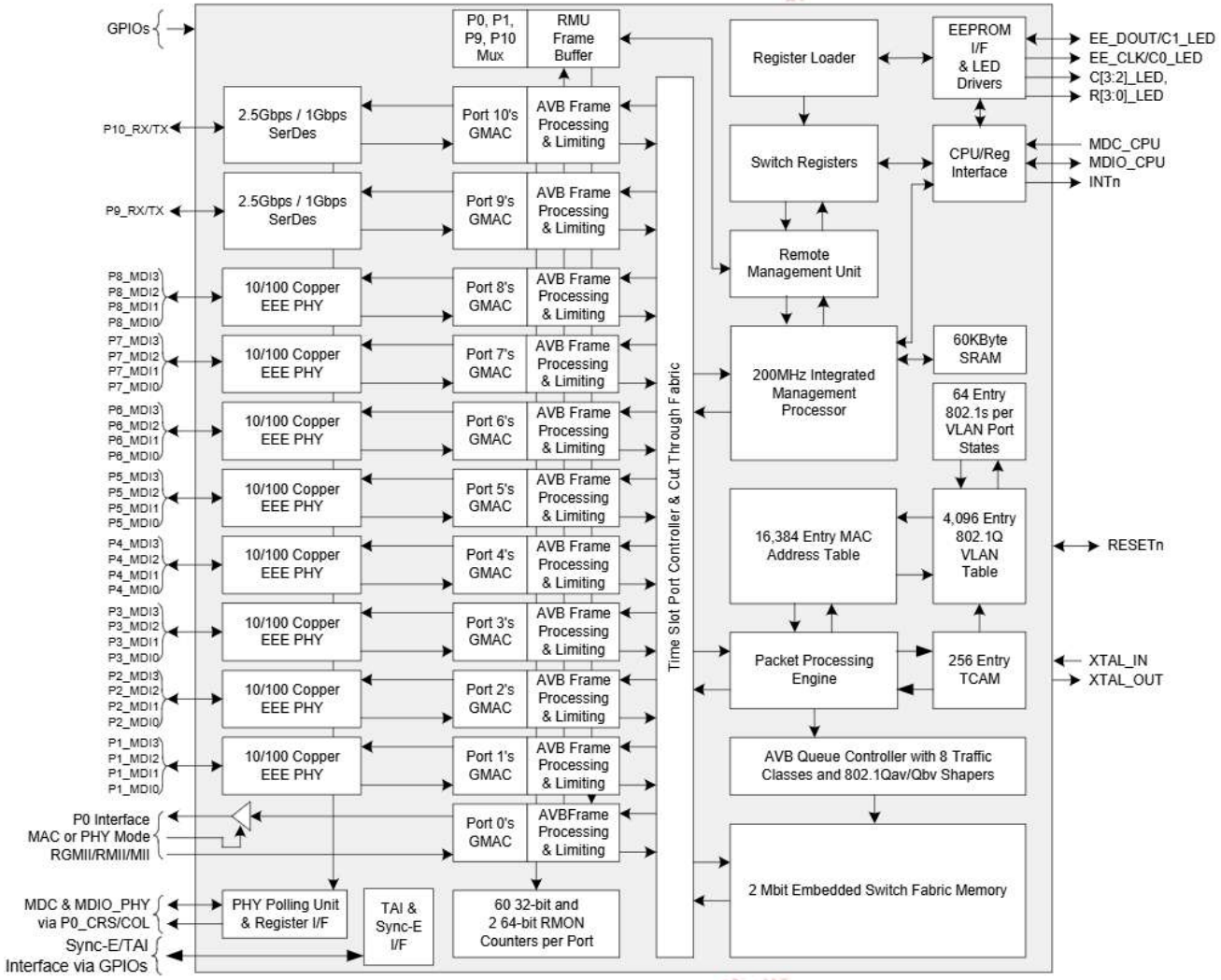


Table of Contents

1 Signal Description 16
1.1 Pin Description 18
1.2 Pin Assignment List 34

2 Application Examples 37
2.1 Managed switch 37
2.1.1 Router Gateway 39
2.2 Device Physical Interfaces 40
2.2.1 Port 0 Configuration Options 40
2.2.2 MII MAC Mode 41
2.2.3 MII PHY Mode 42
2.2.4 MII 200 Mbps Mode 42
2.2.5 RGMII Mode 43
2.2.6 RMII MAC Mode 44
2.2.7 RMII PHY Mode 45
2.2.8 1000BASE-T PHY Interface 45
2.2.9 SERDES modes 45
2.2.10 SGMII MAC or PHY Mode 46
2.2.11 1000BASE-X 46
2.2.12 Port Status Registers 46
2.2.13 PHY Polling Unit (PPU) 46
2.3 General Purpose I/O (GPIO) Configuration 47
2.3.1 Configuring GPIO as a Port Enable Pin 48
2.4 LED Interface 49
2.4.1 LED Options 51
2.4.2 Special LEDs 52
2.5 Connection of external PHYs 53
2.5.1 Connection to 1000BASE-T PHY 53

3 Electrical Specifications 54
3.1 Absolute Maximum Ratings 54
3.1.1 Power Supply Sequencing 55
3.2 Recommended Operating Conditions 55
3.3 Thermal Conditions 56
3.3.1 Thermal Conditions for the 88E6390/88E6190/88E6290 device 144-pin QFP Package 56
3.4 Current Consumption 57
3.5 DC Electrical Characteristics 61
3.5.1 Digital Operating Conditions 61
3.5.2 SGMII Interface 62
3.6 AC Electrical Specifications 67
3.6.1 Reset and Configuration Timing 67
3.6.2 Clock Timing 68

3.7 MII Timing 69
3.7.1 MII PHY Mode Receive Timing - 100 Mbps 69
3.7.2 MII PHY Mode Transmit Timing - 100 Mbps 70
3.7.3 MII MAC Mode Receive Timing 71
3.7.4 MII MAC Mode Transmit Timing 72
3.7.5 TMII PHY Mode Receive Timing - 200 Mbps 73
3.7.6 TMII PHY Mode Transmit Timing - 200 Mbps 74
3.7.7 TMII MAC Mode Clock Timing - 200 Mbps 75
3.7.8 TMII MAC Mode Receive Timing - 200 Mbps 76
3.7.9 TMII MAC Mode Transmit Timing - 200 Mbps 77
3.8 SGMII Timing 78
3.8.1 SGMII Output AC Characteristics 78
3.8.2 SGMII Input AC Characteristics 78
3.9 RGMII Timing 79
3.9.1 RGMII Timing for Different RGMII Modes 80
3.10 RMII Timing 82
3.10.1 RMII Receive Timing 82
3.10.2 RMII Transmit Timing 83
3.11 Serial Management Interface (SMI) Timing 84
3.11.1 SMI Clock Timing (CPU Set) 84
3.11.2 SMI Data Timing (CPU Set) 85
3.11.3 SMI Timing (PHY Set) 86
3.12 2500BASE-X 87
3.12.1 2500BASE-X Characteristics 87
3.13 EEPROM Timing 89
3.13.1 2-Wire EEPROM Timing 89
3.13.2 IEEE AC Transceiver Parameters 91

4 Mechanical Drawing 92

5 Part Order Numbering/Package Marking 94

5.1 Part Order Numbering 94
5.2 Package Marking 95
5.2.1 Industrial Package Marking 95
5.2.2 Commercial Package Marking 96

A Revision History 97

List of Tables

Table 1: 88E6390/88E6190/88E6290 Device Differences 6
Table 2: Network 1G/2.5G SERDES Interface (Ports 9 to 10) 18
Table 3: Network 10/100/1000 PHY Interface (Ports 1 to 8) 19
Table 4: Reference, Clock and Reset 21
Table 5: Port Status LEDs 22
Table 6: Port 0 xMII Receive Interface 25
Table 7: Port 0 xMII Transmit Interface 28
Table 8: GPIO 30
Table 9: System & Register Access 31
Table 10: Power & Ground 32
Table 11: No Connect 33
Table 12: Pin List—Alphabetical by Signal Name 34
Table 13: 88E6390,88E6190 Interface summary 40
Table 14: 88E6290 Interface summary 40
Table 15: Port 0 Configuration Summary 40
Table 16: Port 0 GPIO Assignments 47
Table 17: LED Mapping 49
Table 18: Port 1-8 Hardware Reset LED configuration 52
Table 19: Port 9 Hardware Reset LED configuration 52
Table 20: Port 10 Hardware Reset LED configuration 52
Table 21: Absolute Maximum Ratings 54
Table 22: Recommended Operating Conditions 55
Table 23: 88E6390/88E6190/88E6290 Device Current Consumption 57
Table 24: Digital Operating Conditions 61
Table 25: Programming SGMII Output Amplitude 62
Table 26: Reset and Configuration 67
Table 27: IEEE DC Transceiver Parameters 68
Table 28: MII PHY Mode Receive Timing 69
Table 29: MII PHY Mode Transmit Timing 70
Table 30: MII Receive Timing - MAC Mode 71
Table 31: MII MAC Mode Transmit Timing 72
Table 32: TMII PHY Mode Receive Timing - 200 Mbps 73
Table 33: TMII PHY Mode Transmit Timing - 200 Mbps 74
Table 34: TMII MAC Mode Clock Timing - 200 Mbps 75
Table 35: TMII MAC Mode Receive Timing - 200 Mbps 76
Table 36: TMII MAC Transmit Timing - 200 Mbps 77
Table 37: RGMII Interface Timing 79
Table 38: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 0 80
Table 39: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 1 80

Table 40: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 0 81
Table 41: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 1 81
Table 42: RMII Receive Timing using INCLK 82
Table 43: RMII Transmit Timing using INCLK 83
Table 44: SMI Clock Timing (CPU Set) 84
Table 45: SMI Clock Timing (CPU Set) 85
Table 46: SMI Clock Timing (PHY Set) 86
Table 47: 2500BASE-X Characteristics 87
Table 48: Receiver Input Parameters 88
Table 49: 2-Wire EEPROM Input Timing 89
Table 50: 2-Wire EEPROM Output Timing 90
Table 51: 144-pin E-PAD TQFP (16x16 mm) Package Dimensions 93
Table 52: 88E6390/88E6190/88E6290 Part Order Options 94
Table 53: Revision History 97

List of Figures

Figure 1: 88E6390 Block Diagram 7
Figure 2: 88E6190 Block Diagram 8
Figure 3: 88E6290 Block Diagram 9
Figure 4: 88E6190 and 88E390 144-Pin QFP Pinout 16
Figure 5: 88E6290 144-Pin QFP Pinout 17
Figure 6: Managed Switch 8GE Plus 2 SFP ports 38
Figure 7: Service or Access router 39
Figure 8: MII MAC Mode 41
Figure 9: MII PHY Interface Pins 42
Figure 10: RGMII Interface Pins 43
Figure 11: RMII MAC Interface Pins 44
Figure 12: RMII PHY Interface 45
Figure 13: GPIO Enable Example 48
Figure 14: LEDs plus 2 wire EEPROM 50
Figure 15: Typical SGMII connection to external PHY connections 53
Figure 16: Typical external 10G PHY connection 53
Figure 17: CML I/Os 63
Figure 18: AC connections (CML or LVDS receiver) or DC connection LVDS receiver 64
Figure 19: DC connection to a CML receiver 65
Figure 20: Input Differential Hysteresis 66
Figure 21: Reset and Configuration Timing 67
Figure 22: Oscillator Clock Timing 68
Figure 23: MII PHY Mode Receive Timing 69
Figure 24: MII PHY Mode Transmit Timing 70
Figure 25: MII MAC Mode Receive Timing 71
Figure 26: MII MAC Mode Transmit Timing 72
Figure 27: TMII PHY Mode Receive Timing - 200 Mbps 73
Figure 28: TMII PHY Mode Transmit Timing - 200 Mbps 74
Figure 29: TMII MAC Clock Timing - 200 Mbps 75
Figure 30: TMII MAC Mode Receive Timing - 200 Mbps 76
Figure 31: TMII MAC Mode Transmit Timing - 200 Mbps 77
Figure 32: Serial Interface Rise and Fall Times 78
Figure 33: RGMII Multiplexing and Timing 79
Figure 34: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 0 80
Figure 35: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 1 80
Figure 36: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (bit 4) = 0 81
Figure 37: Receive - RXC Timing when RGMII Receive Delay Control (bit 4) = 1 81
Figure 38: RMII Receive Timing using OUTCLK 82
Figure 39: RMII Transmit Timing using OUTCLK 83

Figure 40: SMI Clock Timing (CPU Set) 84
Figure 41: SMI Data Timing 85
Figure 42: SMI Timing Output (PHY Mode) 86
Figure 43: SMI Timing Input (PHY Mode) 86
Figure 44: Driver Output Voltage Limits and Definitions 87
Figure 45: High-Speed I/O AC Coupled Mode 88
Figure 46: 2-Wire Input Timing 89
Figure 47: 2-Wire EEPROM Output Timing 90
Figure 48: 144-pin E-PAD TQFP (16x16 mm) Mechanical Drawing 92
Figure 49: Sample Part Number 94
Figure 50: 88E6390 and 88E6290 Industrial Package Marking and Pin 1 Location 95
Figure 51: Commercial Package Marking and Pin 1 Location 96

1 Signal Description

Figure 4: 88E6190 and 88E390 144-Pin QFP Pinout

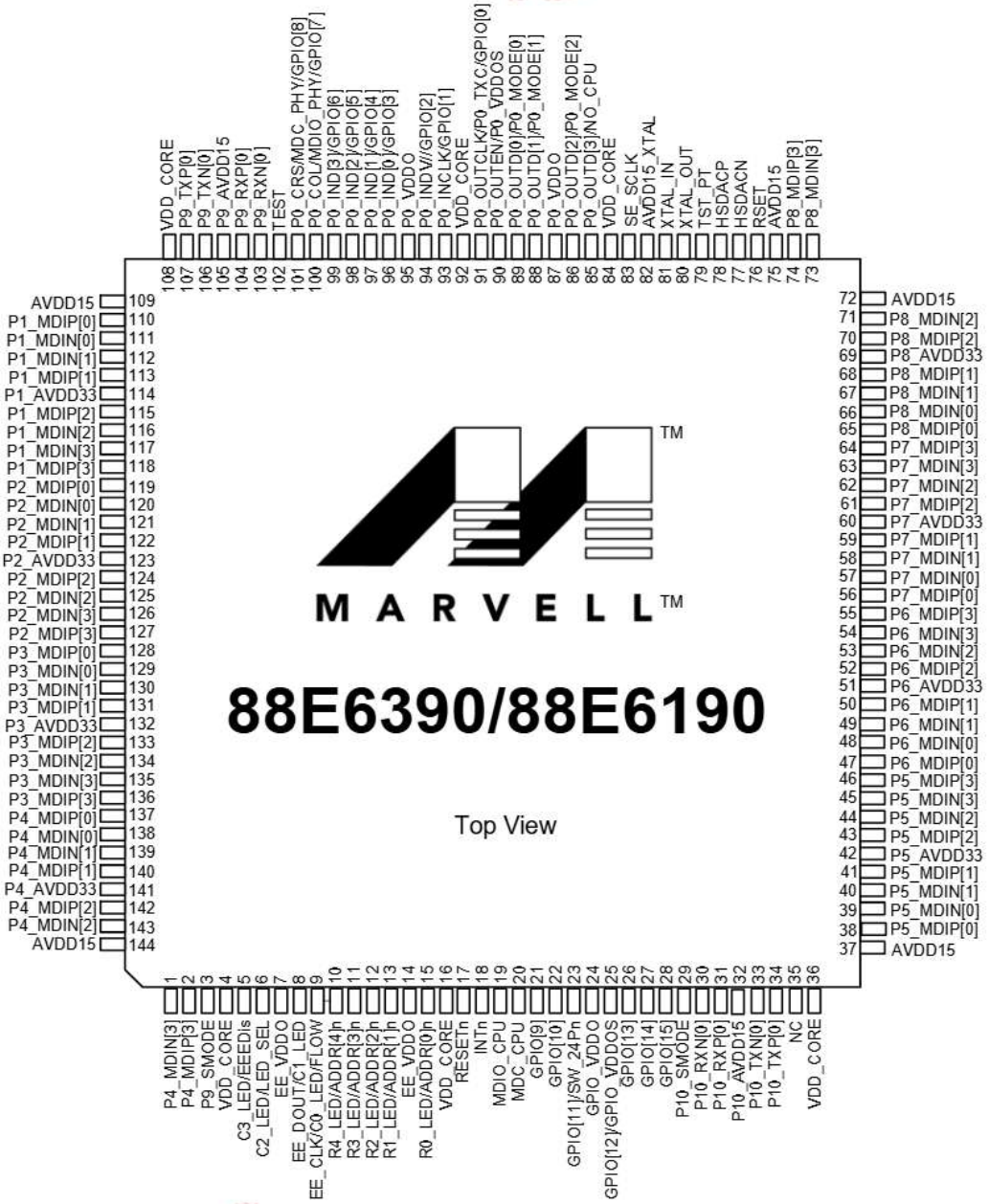
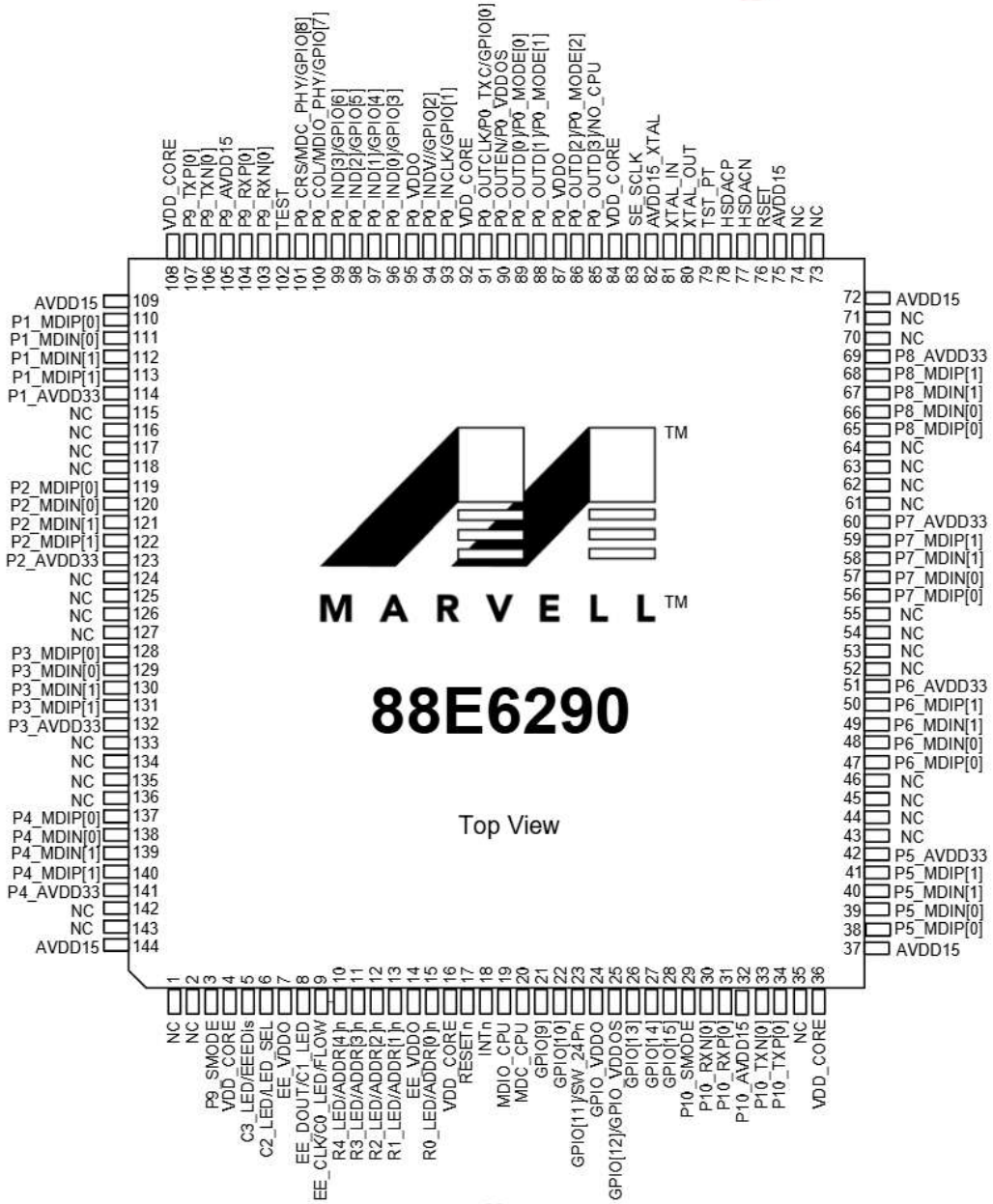


Figure 5: 88E6290 144-Pin QFP Pinout



1.1 Pin Description

Table 2: Network 1G/2.5G SERDES Interface (Ports 9 to 10)

Pin #	Pin Name	Type	Description
31 104	P10_RXP[0] P9_RXP[0]	Input	Receiver input – Positive. Px_RXP[0] connects directly to the fiber-optic receiver's positive output or to another device's TXP (Transmitter output – Positive) pins. Connections to other devices require capacitor isolation.
30 103	P10_RXN[0] P9_RXN[0]	Input	Receiver input – Negative. Px_RXN[0] connects directly to the fiber-optic receiver's negative output or to another device's TXN (Transmitter output – Negative) pins. Connections to other devices require capacitor isolation.
34 107	P10_TXP[0] P9_TXP[0]	Output	Transmitter output – Positive. Px_TXP[0] connects directly to the fiber-optic transmitter's positive input or to another device's RXP (Receiver input – Positive) pins. Connections to other devices require capacitor isolation.
33 106	P10_TXN[0] P9_TXN[0]	Output	Transmitter output – Negative. Px_TXN[0] connects directly to the fiber-optic transmitter's negative input or to another device's RXN (Receiver input – Negative) pins. Connections to other devices require capacitor isolation.

Note This device supports internal terminated media pins. They must be left floating if they are unused.

Table 3: Network 10/100/1000 PHY Interface (Ports 1 to 8)

Pin #	Pin Name	Type	Description
65 56 47 38 137 128 119 110 66 57 48 39 138 129 120 111	P8_MDIP[0] P7_MDIP[0] P6_MDIP[0] P5_MDIP[0] P4_MDIP[0] P3_MDIP[0] P2_MDIP[0] P1_MDIP[0] P8_MDIN[0] P7_MDIN[0] P6_MDIN[0] P5_MDIN[0] P4_MDIN[0] P3_MDIN[0] P2_MDIN[0] P1_MDIN[0]	Input/Output	Media Dependent Interface [0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] corresponds to BI_DA±. In MDIX configuration, MDIP/N[0] corresponds to BI_DB±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. MDIP/N[0] must be left floating if not used.
68 59 50 41 140 131 122 113 67 58 49 40 139 130 121 112	P8_MDIP[1] P7_MDIP[1] P6_MDIP[1] P5_MDIP[1] P4_MDIP[1] P3_MDIP[1] P2_MDIP[1] P1_MDIP[1] P8_MDIN[1] P7_MDIN[1] P6_MDIN[1] P5_MDIN[1] P4_MDIN[1] P3_MDIN[1] P2_MDIN[1] P1_MDIN[1]	Input/Output	Media Dependent Interface [1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] corresponds to BI_DB±. In MDIX configuration, MDIP/N[1] corresponds to BI_DA±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. MDIP/N[1] must be left floating if not used.
70 61 52 43 142 133 124 115 71 62 53 44 143 134 125 116	P8_MDIP[2] P7_MDIP[2] P6_MDIP[2] P5_MDIP[2] P4_MDIP[2] P3_MDIP[2] P2_MDIP[2] P1_MDIP[2] P8_MDIN[2] P7_MDIN[2] P6_MDIN[2] P5_MDIN[2] P4_MDIN[2] P3_MDIN[2] P2_MDIN[2] P1_MDIN[2]	Input/Output	Media Dependent Interface [2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] corresponds to BI_DC±. In MDIX configuration, MDIP/N[2] corresponds to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. MDIP/N[2] must be left floating if not used. 88E6290 These signals are NC

Table 3: Network 10/100/1000 PHY Interface (Ports 1 to 8) (Continued)

Pin #	Pin Name	Type	Description
74	P8_MDIP[3]	Input/Output	Media Dependent Interface [3].
64	P7_MDIP[3]		
55	P6_MDIP[3]		In 1000BASE-T mode in MDI configuration, MDIP/N[3] corresponds to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used.
46	P5_MDIP[3]		
2	P4_MDIP[3]		
136	P3_MDIP[3]		
127	P2_MDIP[3]		MDIP/N[3] must be left floating if not used.
118	P1_MDIP[3]		
			88E6290 These pins are NC
73	P8_MDIN[3]		
63	P7_MDIN[3]		
54	P6_MDIN[3]		
45	P5_MDIN[3]		
1	P4_MDIN[3]		
135	P3_MDIN[3]		
126	P2_MDIN[3]		
117	P1_MDIN[3]		

Table 4: Reference, Clock and Reset

Pin #	Pin Name	Type	Description
76	RSET	Analog	Resistor Current reference. A 4.99k ohm 1% resistor is placed between the RSET and VSS. This resistor is used to set an internal bias reference current.
81	XTAL_IN	Input	25 MHz system reference clock input provided from the board. The clock source can come from an external crystal or an external oscillator. This is the only clock required (for small package). Refer to Section Section 3.6.2 for "Clock Timing" timing requirements.
80	XTAL_OUT	Output	System reference clock output provided to the board. This output can only be used to drive an external crystal. It cannot be used to drive external logic. If an external oscillator is used this pin should be left unconnected.
83	SE_SCLK	Input	Synchronous Ethernet Source Clock Conditioner. This is a 25 MHz reference clock which can be used as a synchronous clock input from synchronous Ethernet applications. Each PHY, via a PHY register, can select this clock input as its reference clock input instead of using the default XTAL_IN input. SE_CLK is internally pulled low via a resistor so the pin can be left floating when unused.
17	RESETn	Input	Hardware reset. Active low. The device is configured during reset. When RESETn is low some configuration pins become inputs and the value seen on these pins is latched on the rising edge of RESETn or sometime after. Other configuration pins are active during RESETn low and become inputs after RESETn rises. These pins latch their configuration data sometime after RESETn rises and then these pins become their defined function. Refer to Section 3.6.1 of the AC Electrical Specifications for Reset and Configuration Timing details.

Table 5: Port Status LEDs

Pin #	Pin Name	Type	Description
10 11 12 13 15	R4_LED /ADDR[4]n R3_LED /ADDR[3]n R2_LED /ADDR[2]n R1_LED /ADDR[1]n R0_LED /ADDR[0]n	Typically Output, PU	Parallel multiplexed LED outputs. These active low LED pins directly drive the port's LEDs supporting a range from 1 to 6 LEDs in a multiplexed fashion. In this mode the cathode of each LED connects to these pins through a series current limiting resistor. The anode of each LED connects to one of the Cx_LED pins below Section 2.4 for LED applications. The LEDs can be configured to display many options (refer to Section 2.4.1). All LEDs are turned on whenever RESETn is low so their functionally can be visually verified during PCB manufacturing testing. Rx_LED are multifunction pins which are used to configure the device after a hardware reset. After reset is asserted, the Rx_LED pins become inputs and the configuration information below is latched 1 mSec after the rising edge of RESETn as follows: ADDR[4:0]n sets the device's SMI address. Note: The inverted values 'seen' on these CONFIG pins are used as the SMI address.When ADDR[4:0]n are left floating or pulled high the device will be configured in single chip addressing mode. In single chip addressing mode the SMI bus can not be shared with other devices. When SMI bus is to be shared with other devices the SMI address of this device must be a none 0 zero value. To configure this device as SMI address 0x01 ADDR[4:0]n should be 0x1E. To configure the device as SMI address 0x1E ADDR[4:0]n should be 0x01.
8	EE_DOUT /C1_LED	Input/Output, PU	Serial EEPROM data I/O to/from a 2-wire EEPROM device and Column 0 for the LEDs. EE_DOUT is serial EEPROM data referenced to EE_CLK used to receive and send the EEPROM address/data to/from the external serial EEPROM (if present). 2-wire EEPROMs require that this pin is connected to EE_VDDO through a pull-up resistor. EE_DOUT is internally pulled high via a resistor so the pin can be left floating when unused.

Table 5: Port Status LEDs (Continued)

Pin #	Pin Name	Type	Description
9	EE_CLK /C0_LED /FLOW	Typically Output, PD	Serial EEPROM clock and column 1 for the LEDs. EE_CLK is the serial EEPROM clock reference output by the devices. It is used to shift the external serial EEPROM (if installed) to the next data bit so the default values of the internal registers can be overridden. EE_CLK is a multi-function pin which is also used to connect to the anode of LED column 1 for each row, if used in the multiplexed LED mode (see R[3:0]_LED above). It is also used to configure the device after a hardware reset. After reset is asserted, EE_CLK becomes an input and the FLOW configuration information below is latched 1 mSec after the rising edge of RESETn as follows: 0x0 = Disable flow control on all ports 0x1 = Enable advertisement of full-duplex flow control on all PHYs and enable "forced collision" flow control on all half duplex ports Full-duplex flow control requires support from the end station. It is supported on any full-duplex port that has Auto-Negotiation enabled, advertises that it supports Pause (i.e., FLOW = 1 at reset), and sees that the end station also supports Pause (from data returned during Auto-Negotiation). Half-duplex flow control is active on all half-duplex ports when enabled. Note: The inverted values 'seen' on these CONFIG pins are use by internal logic. EE_CLK is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7K ohm resistor to EE_VDDO for a configuration high.
6	C2_LED /LED_SEL	Typically Output, PD	C2_LED is a multi-function pin which is used to connect to the anode of LED column 2 for each row, if used in the multiplexed LED mode (see R[3:0]_LED above). It is also used to configure the device after a hardware reset. After reset is asserted, C2_LED becomes an input and the LED_SEL configuration information below is latched 1 mSec after the rising edge of RESETn as follows: 0 = Link/Activity w/ Speed by 3 Color 1 = Link/Activity w/ Separate Speed LED C2_LED is internally pulled low via a resistor so the pin can be left floating when unused.

Table 5: Port Status LEDs (Continued)

Pin #	Pin Name	Type	Description
5	C3_LED /EEEDis	Typically Output, PD	C3_LED is a multi-function pin which is used to connect to the anode of LED column 3 for each row, if used in the multiplexed LED mode (see R[4:0]_LED above). It is also used to configure the device after a hardware reset. After reset is asserted, C3_LED becomes an input and the EEEDis configuration information below is latched 1 mSec after the rising edge of RESETn as follows: 0 = Advertise Energy Efficient Ethernet (EEE) in the PHYs. 1 = Do not advertise Energy Efficient Ethernet (EEE) in the PHYs. C3_LED is internally pulled low via a resistor so the pin can be left floating when unused.

Table 6: Port 0 xMII Receive Interface

Pin #	Pin Name	Type	Description
93	P0_INCLK /GPIO[1]	Input/Output, PU	Input Clock. INCLK is a reference for INDV and IND. The speed of INCLK is expected to be 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depending upon the speed of the port. In RGMII mode INCLK is used as RXC. INCLK is an output when the xMII is configured in a PHY mode (when the port's Px_MODE = 0x0, or 0x1) or when it is a GPIO pin which is configured to be an output. When the port is in RMII mode or disabled (by its Px_MODE = 0x4, 0x5 or 0x6) this pin becomes GPIO[1] and becomes an input. INCLK is tri-stated during RESETns and it is internally pulled high so the pin can be left floating when unused.
94	P0_INDV /GPIO[2]	Input, PD	Input Data Valid. Input Data Valid is used to indicate when IND[3:0] (or IND[1:0] where appropriate) contains frame information. INDV must be synchronous to INCLK for all modes except for RMII modes where INDV must be synchronous to OUTCLK. In RGMII mode INDV is used as RX_CTL. When this port is disabled (by its P0_MODE = 0x6) this pin becomes GPIO[2]. INDV is internally pulled low via resistor so the pin can be left floating when unused.
99 98 97 96	P0_IND[3] /GPIO[6] P0_IND[2] /GPIO[5] P0_IND[1] /GPIO[4] P0_IND[0] /GPIO[3]	Input, PU	Input Data. IND[3:0] (or IND[1:0] where appropriate) receives the data to be sent into the switch. IND must be synchronous to INCLK for all modes except for RMII modes. In MII, 200BASE, 100BASE and 10BASE modes IND[3:0] is used. In RMII modes only IND[1:0] are used and they must be synchronous to OUTCLK. In RGMII mode IND[3:0] are used as RXD[3:0]. When this port is disabled (by its P0_MODE = 0x6) these pins becomes GPIO[6:3]. When the port is in RMII mode (by its P0_MODE = 0x4 or 0x5) IND[3:2] become GPIO[6:5]. The IND pins are internally pulled high via resistor so the pins can be left floating when unused.

Table 6: Port 0 xMII Receive Interface (Continued)

Pin #	Pin Name	Type	Description
101	P0_CRS /MDC_PHY /GPIO[8]	Input/Output, PU	Carrier Sense, Management Data Clock, Master, or GPIO[8]. Carrier sense is used to indicate carrier has been detected on the line. CRS is not synchronous to INCLK. CRS is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is CRS when the port's Px_MODE = 0x1 or 0x2. CRS is an output for Px_MODE = 0x1 and it's an input for Px_MODE = 0x2. As a Management Data Clock, in Master mode, this pin is the reference clock output for the serial management interface (SMI) that connects to an external SMI slave device, typically external PHYs. This pin is MDC_PHY when the port's Px_MODE is not 0x1 or 0x2 and the NO_CPU configuration pin was high at the rising edge of RESETn. The Master SMI is used to access registers in any external SMI device (like a PHY) and it is controllable via switch registers. Alternatively, this pin becomes GPIO[8], which supports all functions described in Section 2.3. CRS is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the port's Px_MODE pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P0_ ENABLE.

Table 6: Port 0 xMII Receive Interface (Continued)

Pin #	Pin Name	Type	Description
100	P0_COL /MDIO_PHY /GPIO[7]	Input/Output, PU	Collision, or Management Data I/O, Master, or GPIO[7]. Collision is used to indicate both transmit and receive are occurring at the same time in half duplex mode. COL is not synchronous to INCLK. COL is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is COL when the port's Px_MODE = 0x1 or 0x2. COL is an output for Px_MODE = 0x1 and it's an input for Px_MODE = 0x2. As a Management Data I/O, in Master mode, this pin is used to transfer management data in and out of the device synchronously to MDC_PHY. This pin requires an external pull-up resistor in the range of 4.7K to 10K ohm. This pin is MDIO_PHY when the port's Px_MODE is not 0x1 or 0x2 and the NO_CPU configuration pin was high at the rising edge of RESETn[1]. When NO_CPU is pulled low (CPU_MANAGED) mode, this pin becomes GPIO[7]. When NO_CPU is pulled high (UN-Managed mode) this pin becomes MDC_PHY and connects to an external SMI device such as a PHY. Refer to Section 2.5 for details. When in CPU attached mode, this signal can be re-configured as MDIO_PHY by clearing the NormalSmi bit in the Scratch and Misc registers. COL is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the port's Px_MODE pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P0_ ENABLE.

1. The NO_CPU configuration pin is used to determine the initial function of this pin after reset. The pin's function can be modified by changing a register (NormalSMI bit in Scratch and Misc registers Index 0x01).

Table 7: Port 0 xMII Transmit Interface

Pin #	Pin Name	Type	Description
90	P0_OUTEN /P0_VDDOS	Typically Output, PD	Output Enable. Output enable is used to indicate when OUTD[3:0] or OUTD[1:0] contains frame information. OUTEN is synchronous to OUTCLK in all modes. In RGMII mode OUTEN is used as TX_CTL. P0_OUTEN is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the configuration information below is latched at the rising edge of RESETn: P0_VDDOS 1 = The P0_VDDO pins are powered by 2.5 volts P0_OUTEN is tri-stated during RESETn or when P0_ ENABLE is low. OUTEN is internally pulled low via resistor so the pin can be left floating when unused. Use a 4.7K ohm resistor to P0_VDDO for a configuration high.
91	P0_OUTCLK /P0_TXC /GPIO[0]	Input/Output, PU	Output Clock. OUTCLK is a clock reference for OUTEN and OUTD[3:0]. The speed of OUTCLK is 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depends on the speed of the Port. The direction of OUTCLK is a function of the port's Px_MODE (Port offset 0x00). See the C_Mode register bits in Port offset 0x00. In RGMII mode OUTCLK is used as TXC. In RMII mode OUTCLK is used as REFCLK. When this port is disabled (by its Px_MODE = 0x6) this pin becomes GPIO[0]. OUTCLK is internally pulled high via resistor so the pin can be left floating when unused.

Table 7: Port 0 xMII Transmit Interface (Continued)

Pin #	Pin Name	Type	Description
85	P0_OUTD[3] /NO_CPU	Typically Output, PU_	Output Data. OUTD[3:0] (or OUTD[1:0] where appropriate) outputs the data to be transmitted from the switch. OUTD is synchronous to OUTCLK in all modes. In RGMII mode OUTD[3:0] are used as TXD[3:0]. In RMII mode OUTD[1:0] are used and OUTD[3:2] are tri-stated. P0_OUTD are multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn as follows: OUTD[3] = No CPU OUTD[2:0] = P0_MODE[2:0] No CPU selects the flow control setting as follows: 0 = CPU is attached 1 = No CPU is attached When the 'CPU is attached' mode is selected, all the ports will be initialized in the Disabled Port State and the PHYs will be powered down. This allows software time to boot and fully configure the switch before it allows packets to flow through it. Whenever the switch is used with a CPU, the 'CPU is attached' mode must be used. P0_MODE[2:0] sets Port 0's Mode of operation as follows: 0x0 = Full Duplex Only MII PHY Mode[1] 0x1 = MII PHY mode w/output MII CLKs[2] at 2.5, 25 or 50 MHz[3] 0x2 = MII MAC mode w/input MII CLKs 0x3 = Reserved for future use 0x4 = RMII PHY mode w/output P0_OUTCLK at 50 MHz 0x5 = RMII MAC mode w/input P0_OUTCLKs at 50 MHz 0x6 = Port disabled (with its pins tri-stated)[4] 0x7 = RGMII mode P0_OUTD pins are tri-stated during RESETn or when P0_ ENABLE is low. OUTD pins are internally pulled high via resistor so the pins can be left floating when unused. Use a 4.7K ohm resistor to VSS for a configuration low.
86	P0_OUTD[2] /P0_MODE[2]		
88	P0_OUTD[1] /P0_MODE[1]		
89	P0_OUTD[0] /P0_MODE[0]		

1. This mode is identical to P0_MODE 0x1 except the P0_CRS and P0_COL pins are used for other functions.
2. P0's MII CLKs refer to both P0_OUTCLK and P0_INCLK.
3. P0_OUTCLK's frequency is determined by the port's ForceSpd and AltSpeed bits (Port offset 0x01).
4. In this mode many of P0's pins become GPIO pins.

Table 8: GPIO

Pin #	Pin Name	Type	Description
21 22	GPIO[9] GPIO[10]	Input/Output, PU	General Purpose I/O pins. GPIO[15:9] are general purpose input/output pins whose direction and data is controllable via switch registers GPIO[12:11] are the multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn: GPIO[11] = SW_24Pn GPIO[12] = GPIO_VDDOS SW_24Pn 0x0 = Configures the device for cascading mode Cross-chip SERDES on Port 9, and 10 interfaces. Separate Port Based VLAN between Port 9 and Port 10 Enable configuration of Learn2All Set FrameMode to DSA mode for Port 9 and Port 10 Force link up for Port 9 and Port 10 Use this mode for a 3 chip ring only. 0x1 = Normal operation GPIO_VDDOS 1 = The GPIO_VDDO pins are powered by 2.5V See EE_VDDO for the list of pins that are powered by this rail. GPIO[15:9] pins are internally pulled high via resistor so the pins can be left floating when unused. Use a 4.7K ohm resistor to VSS for a configuration GPIO[12:11] low.
23 25 26 27 28	GPIO[11] /SW_24Pn GPIO[12] /GPIO_VDDOS GPIO[13] GPIO[14] GPIO[15]		
3 29	P9_SMODE P10_SMODE	Input, PU	Px_SMODE are pins to configure the device for sets the Port's SERDES Mode of operation as follows 0x0 = 2.5 Gbps Operation 0x1 = SGMII/1000X Operation base on PHYDETECT bit in port status register. Px_SMODE pins are internally pulled high via resistor so the pins can be left floating when unused. Use a 4.7K ohm resistor to VSS for a configuration low.

Table 9: System & Register Access

Pin #	Pin Name	Type	Description
20	MDC_CPU	Input	Management Data Clock, Slave. MDC_CPU is the reference clock input for the serial management interface (SMI) that connects to an external SMI master, typically a CPU. A continuous clock stream is not expected. The maximum frequency supported is 20.0 MHz The CPU's SMI interface is used to access the device's registers but it cannot be used until the device's INTn pin becomes active low (indicating the Register Loader is done processing the EEPROM or that no EEPROM was present). MDC_CPU is internally pulled high via a resistor so it can be left floating when unused. **NOTE:** MDC_CPU is powered by the GPIO_VDDO pins.
19	MDIO_CPU	Input/Output	Management Data I/O, Slave. MDIO_CPU is used to transfer management data in and out of the device synchronously to MDC_CPU. This pin requires an external pull-up resistor in the range of 4.7K to 10K Ω. The device uses one or all of the 32 possible SMI port addresses (two modes are supported). The address(es) that are used are selectable using the Rx_LED/ADDRn configuration pins. MDIO_CPU is internally pulled high via a resistor so it can be left floating when unused. **NOTE:** MDIO_CPU is powered by the GPIO_VDDO pins.
18	INTn	Input/Open Drain Output	INTn is an active low, open drain pin that is asserted to indicate an unmasked interrupt event occurred. A single external pull-up resistor is required somewhere on this interrupt net for it to go high when it is inactive. The INTn pin will go active low which indicates the SMI interface (MDC_CPU/MDIO_CPU pins) is available for use.
102	TEST	Input, PD	Test Input. Test is used to place the chip into its manufacturing test modes. Do not connect this pin to anything other than VSS or improper device operation will result. Test should be pulled or tied low.
78 77	HSDACP HSDACN	O	AC Test Points (Positive and Negative). The HSDACP/N outputs are used for AC Test Points. These pins must be connected to a 50 ohm termination resistor to VSS. These pins can be left floating if not used for clock cascade, IEEE testing, and debug test points are not of importance.
79	TST_PT	O	DC Test Point. The TST_PT pin should be left floating if not used.

Table 10: Power & Ground

Pin #	Pin Name	Type	Description
87 95	P0_VDDO	Power	Power to Port 0's interface. P0_VDDO must be connected to: 2.5V for 2.5V I/O or 1.8V for 1.8V I/O (and P0_VDDOS must be configured accordingly – see P0_OUTEN). 1.8V configuration will be automatically detected by internal voltage sensing logic.
7 14	EE_VDDO	Power	Power to LED, EEPROM interface and the RESETn pin. EE_VDDO must be connected to 3.3V for 3.3V I/O.
24	GPIO_VDDO	Power	Power to GPIO[15:9], MDC_CPU, and MDIO_CPU interface pins. GPIO_VDDO must be connected to: 2.5V for 2.5V I/O or 1.8V for 1.8V I/O (and GPIO_VDDOS must be configured accordingly – see GPIO[12]). 1.8V configuration will be automatically detected by internal voltage sensing logic.
69 60 51 42 141 132 123 114	P[8:1]_AVDD33	Power	3.3V power to analog core used to power each Gig PHY interface.
37 72 75 109 144	AVDD15	Power	1.5V power to analog core.
32 105	P[10:9]_AVDD15	Power	1.5V power to analog core used to power the SERDES interface.
82	AVDD15_XTAL	Power	1.5V power to analog core used to power on-chip XTAL.
4 16 36 84 92 108	VDD_CORE	Power	Power to digital core. 1.05 for Commercial temp operation 1.1 for Industrial temp operation. Industrial temp operation requires industrial temperature part number. For details, refer to Table 52, 88E6390/88E6190/88E6290 Part Order Options, on page 94.
E-PAD	VSS	Ground	Ground to the device. The device is packaged in the 144 pin package with an E-PAD (exposed die pad) on the bottom of the package. This E-PAD must be soldered to VSS as it is the main VSS connection on the device.

Table 11: No Connect

Pin #	Pin Name	Type	Description
35	NC	-	No Connect. Do not connect this pin to anything. This pin must be left unconnected.

1.2 Pin Assignment List

Table 12: Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
37	AVDD15
72	AVDD15
75	AVDD15
109	AVDD15
144	AVDD15
82	AVDD15_XTAL
6	C2_LED/LED_SEL
5	C3_LED/EEEDis
9	EE_CLK/C0_LED/FLOW
8	EE_DOUT/C1_LED
7	EE_VDDO
14	EE_VDDO
22	GPIO[10]
23	GPIO[11]/SW_24Pn
25	GPIO[12]/GPIO_VDDOS
26	GPIO[13]
27	GPIO[14]
28	GPIO[15]
21	GPIO[9]
24	GPIO_VDDO
77	HSDACN
78	HSDACP
18	INTn
20	MDC_CPU
19	MDIO_CPU
35	NC
100	P0_COL/MDIO_PHY/GPIO[7]
101	P0_CRS/MDC_PHY/GPIO[8]

Pin Number	Pin Name
93	P0_INCLK/GPIO[1]
96	P0_IND[0]/GPIO[3]
97	P0_IND[1]/GPIO[4]
98	P0_IND[2]/GPIO[5]
99	P0_IND[3]/GPIO[6]
94	P0_INDV/GPIO[2]
91	P0_OUTCLK/P0_TXC/GPIO[0]
89	P0_OUTD[0]/P0_MODE[0]
88	P0_OUTD[1]/P0_MODE[1]
86	P0_OUTD[2]/P0_MODE[2]
85	P0_OUTD[3]/NO_CPU
90	P0_OUTEN/P0_VDDOS
87	P0_VDDO
95	P0_VDDO
114	P1_AVDD33
111	P1_MDIN[0]
112	P1_MDIN[1]
116	P1_MDIN[2]
117	P1_MDIN[3]
110	P1_MDIP[0]
113	P1_MDIP[1]
115	P1_MDIP[2]
118	P1_MDIP[3]
123	P2_AVDD33
120	P2_MDIN[0]
121	P2_MDIN[1]
125	P2_MDIN[2]
126	P2_MDIN[3]

Pin Number	Pin Name
119	P2_MDIP[0]
122	P2_MDIP[1]
124	P2_MDIP[2]
127	P2_MDIP[3]
132	P3_AVDD33
129	P3_MDIN[0]
130	P3_MDIN[1]
134	P3_MDIN[2]
135	P3_MDIN[3]
128	P3_MDIP[0]
131	P3_MDIP[1]
133	P3_MDIP[2]
136	P3_MDIP[3]
141	P4_AVDD33
138	P4_MDIN[0]
139	P4_MDIN[1]
143	P4_MDIN[2]
1	P4_MDIN[3]
137	P4_MDIP[0]
140	P4_MDIP[1]
142	P4_MDIP[2]
2	P4_MDIP[3]
42	P5_AVDD33
39	P5_MDIN[0]
40	P5_MDIN[1]
44	P5_MDIN[2]
45	P5_MDIN[3]
38	P5_MDIP[0]
41	P5_MDIP[1]

Pin Number	Pin Name
43	P5_MDIP[2]
46	P5_MDIP[3]
51	P6_AVDD33
48	P6_MDIN[0]
49	P6_MDIN[1]
53	P6_MDIN[2]
54	P6_MDIN[3]
47	P6_MDIP[0]
50	P6_MDIP[1]
52	P6_MDIP[2]
55	P6_MDIP[3]
60	P7_AVDD33
57	P7_MDIN[0]
58	P7_MDIN[1]
62	P7_MDIN[2]
63	P7_MDIN[3]
56	P7_MDIP[0]
59	P7_MDIP[1]
61	P7_MDIP[2]
64	P7_MDIP[3]
69	P8_AVDD33
66	P8_MDIN[0]
67	P8_MDIN[1]
71	P8_MDIN[2]
73	P8_MDIN[3]
65	P8_MDIP[0]
68	P8_MDIP[1]
70	P8_MDIP[2]
74	P8_MDIP[3]

Pin Number	Pin Name
105	P9_AVDD15
103	P9_RXN[0]
104	P9_RXP[0]
3	P9_SMODE
106	P9_TXN[0]
107	P9_TXP[0]
32	P10_AVDD15
30	P10_RXN[0]
31	P10_RXP[0]
29	P10_SMODE
33	P10_TXN[0]
34	P10_TXP[0]
15	R0_LED/ADDR[0]n
13	R1_LED/ADDR[1]n
12	R2_LED/ADDR[2]n
11	R3_LED/ADDR[3]n
10	R4_LED/ADDR[4]n
17	RESETn
76	RSET
83	SE_SCLK
102	TEST
79	TST_PT
4	VDD_CORE
16	VDD_CORE
36	VDD_CORE
84	VDD_CORE
92	VDD_CORE
108	VDD_CORE
EPAD	VSS

Pin Number	Pin Name
81	XTAL_IN
80	XTAL_OUT

2 Application Examples

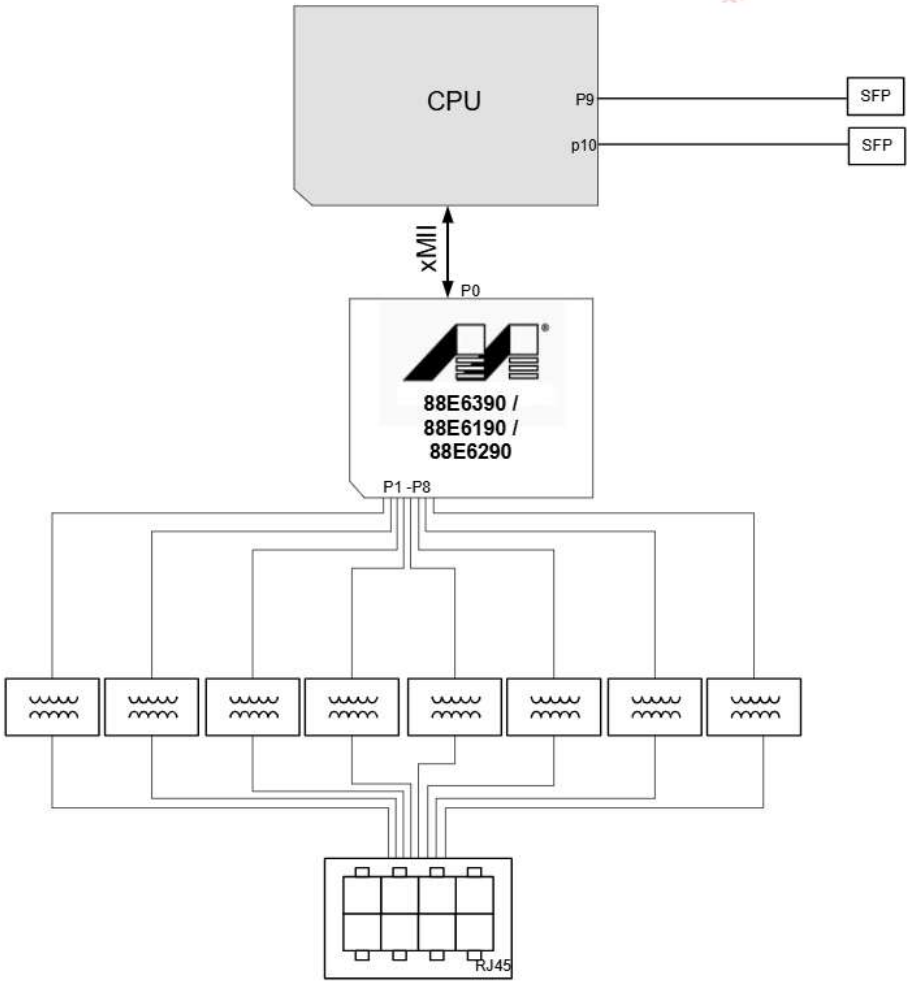
The 88E6390, 88E190 and the 88E6290 have 8 integrated Ethernet Phys, 2 Single lane SERDES ports. and 1 xMII digital port. On the 88E6190 and 88E6390, the integrated PHYs are Trippe speed 1000BASE-T. The 88E6290 the integrated PHYs are Dual speed 100BASE-Tx/10BASE-T. The integrated PHYs are the latest voltage mode PHYS with Energy Efficient Ethernet capabilities. The SERDES ports can emulate 1000BASE-X/SGMII/2.5G modes.

2.1 Managed switch

Figure 6 is an example of how this device can be used in a managed switch application that supports the following interfaces:

- Up to eight PHY ports
- Up to 2 SERDES ports
- 2 (SFP Small Form Plug) cages which can be used for optical transceivers.
- xMII connection to optional management CPU to implement bridge management protocols such as IGMP MLD 802.1X.

Figure 6: Managed Switch 8GE Plus 2 SFP ports

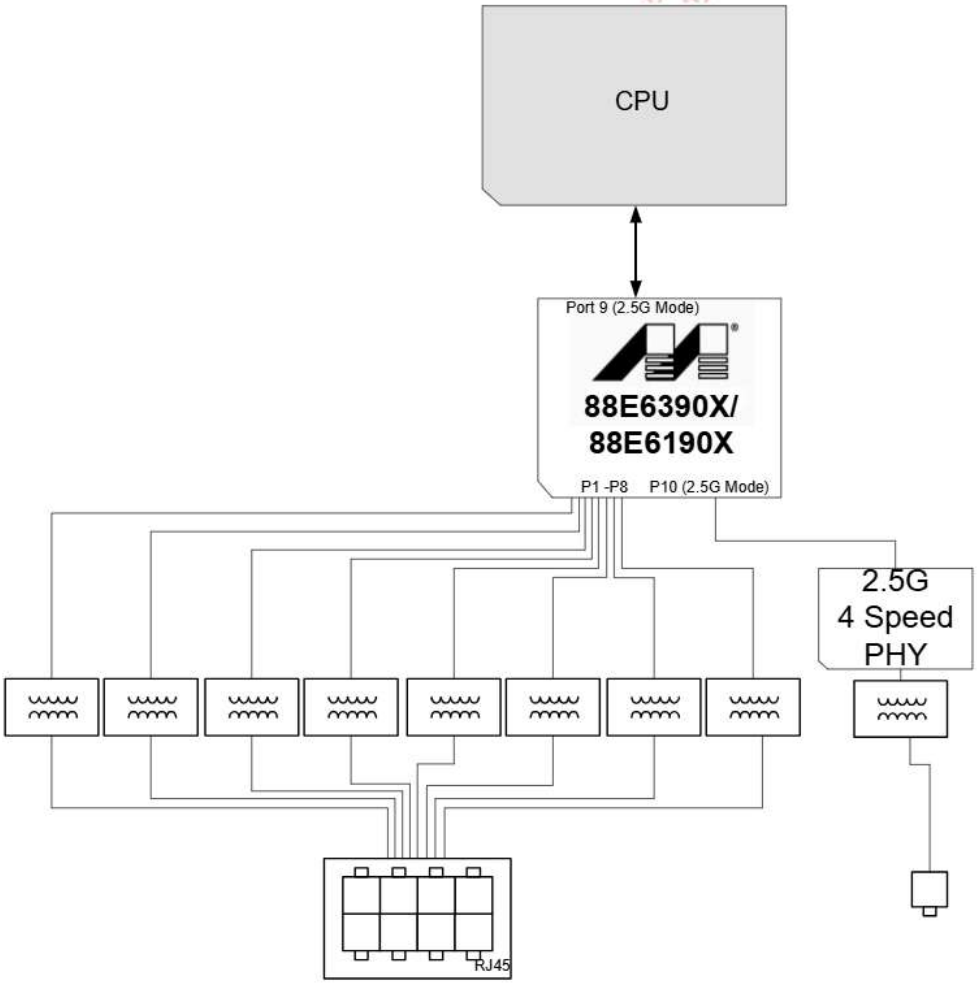


The SFP cages typically accommodate fiber modules. There is no method for the SERDES port to auto detect the type of module inserted. When running 2.5G mode the SFP fiber modules must be rated for the speed.

2.1.1 Router Gateway

In the router gateway application the ports 1-8 are used for LAN. Ports 10 is used for a WAN connection. All LAN and wan traffic can be isolated with port based VLAN ensure that LAN to WAN traffic is routed via the CPU attached to port 10.

Figure 7: Service or Access router



2.2 Device Physical Interfaces

Table 13: 88E6390,88E6190 Interface summary

Port	1000BASE-T (Triple Speed)	RGMII	RMII	MII/ 200 Mbps MII	2.5G	SGMII 1000BASE-X
0		x	x	x		
1-8	x					
9-10					x	x

Table 14: 88E6290 Interface summary

Port	100Base TX (Dual speed)	RGMII	RMII	MII/ 200 Mbps MII	2.5G	SGMII 1000BASE-X
0		x	x	x		
1-8	x					
9-10					x	x

2.2.1 Port 0 Configuration Options

Table 15 indicates all supported port 0 xMII modes. Some unused port 0 pins can be used as GPIO signals.

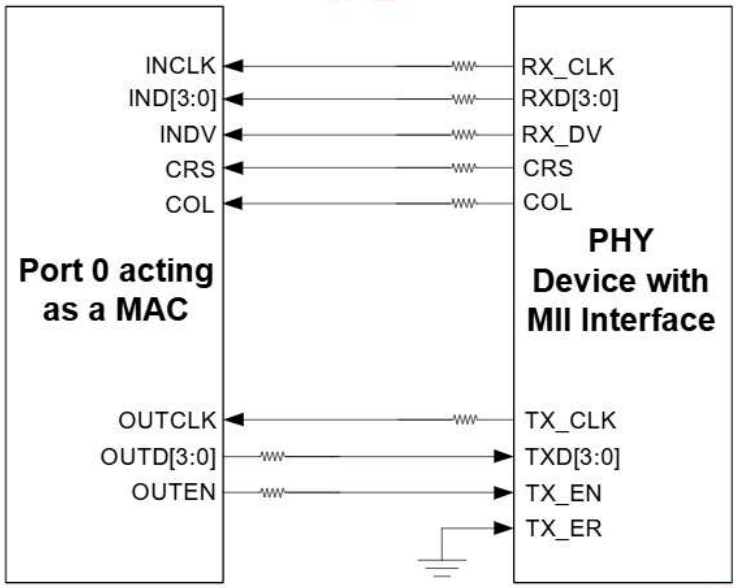
Table 15: Port 0 Configuration Summary

P0_MODE[2:0]	Mode	Notes
000	Full-duplex MII PHY	COL and CRS are not used
001	MII PHY	Supports connection to MAC
010	MII MAC	Supports connection to external PHY type device
100	RMII PHY	OUTCLK = 50 MHZ
101	RMII MAC	OUTCLK is a 50 MHZ input.
110	Disabled	P0 is not used and pins are tri-stated until configured for other functions via register access.
111	RGMII	Supports connection to external CPU and PHY

2.2.2 MII MAC Mode

In MII MAC Mode, sometimes called 'Forward MII mode, P0_INCLK and P0_OUTCLK are inputs. The clock provided by the attached device can be from DC-50 MHz. This mode is typically used to support connections to external PHYs. Figure 8 is an example of MII MAC mode when connected to a device emulating a PHY.

Figure 8: MII MAC Mode



.

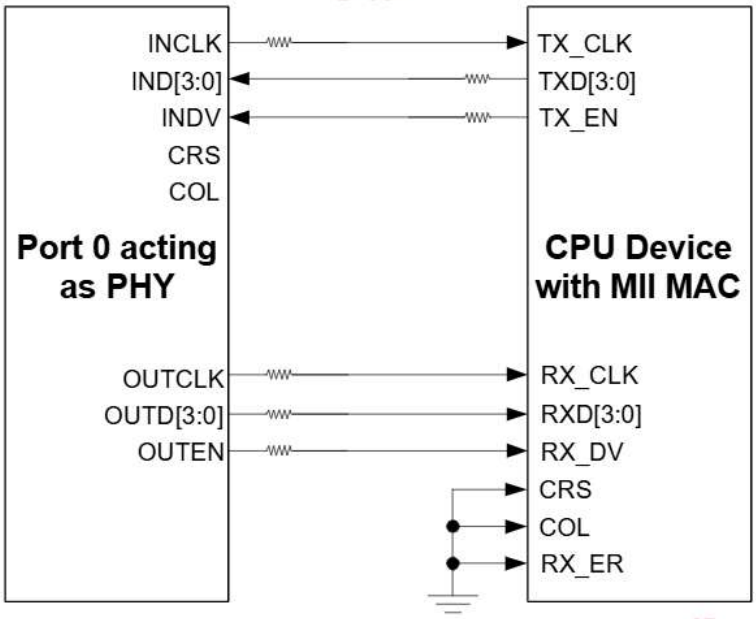
Note If COL and CRS are not used, use a 4.7k pull-down resistor.

Note When configured in MII MAC mode and no clock is provided, the link should be forced down via switch port register 1.

2.2.3 MII PHY Mode

MII PHY Mode is sometimes called 'Reverse MII' mode, This mode is typically used to connect the switch port to a CPU. In this mode, P0_INCLK and P0_OUTCLK are both outputs. Figure 9 is an example of using port 0 MII PHY mode. INCLK and OUTCLK output frequency is 2.5 MHZ for 10 Mbps, 25 MHz for 100 Mbps and 50 MHz in 200 Mbps mode. COL and CRS are only used when operating in half-duplex mode. RX_ER should be tied to ground because the switch does not generate this signal.

Figure 9: MII PHY Interface Pins



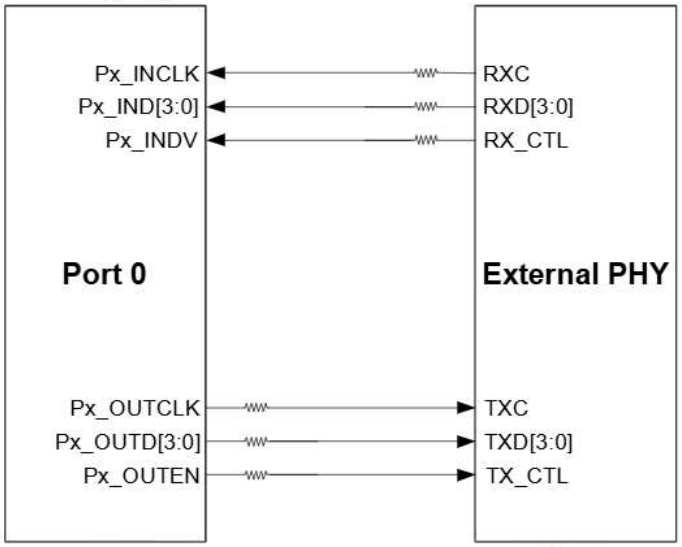
2.2.4 MII 200 Mbps Mode

When port 0 is configured in MII MAC or MII PHY mode, it can configured to run at 200 Mbps mode. This is done via register access. In 200 Mbps mode, the TX/RX clocks run at 50 MHZ.

2.2.5 RGMII Mode

In RGMII Mode, Port 0 emulates a Reduced Gigabit Media Independent Interface (RGMII) so that it can be directly connected to an external RGMII-based Gigabit PHY or CPU. When the RGMII mode is selected, transmit control (P0_OUTEN) is presented on both clock edges of Px_OUTCLK. Receive control (Px_INDV) is presented on both clock edges of Px_INCLK or Px_INCLK. A triple speed interface is supported in RGMII mode (i.e., 10, 100 and 1000). When the PHY completes auto-negotiation and brings the link up, the auto-negotiated speed, duplex and flow control information must be moved from the PHY to the MAC so the MAC matches the PHY's link state. This is done automatically by the PPU if the port's PHYDetect bit is set to a one (Port offset 0x00). The default speed and duplex is 1000 Mbps/full-duplex. The speed can be changed at any time with port register 1. RGMII supports an internal transmit and receive delay mechanism which allows for all traces to be routed at the same length without adding additional timing skew in the board layout. RGMII is a symmetrical interface therefore there is no need for separate MAC/PHY emulation. Refer to Figure 10 for RGMII connections.

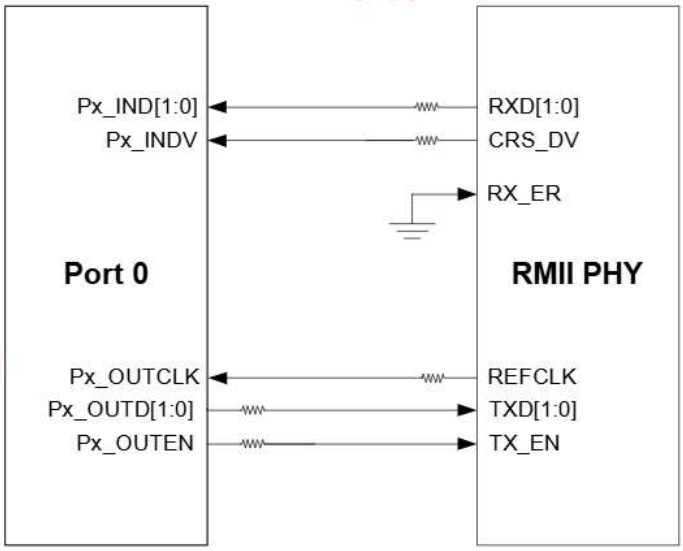
Figure 10: RGMII Interface Pins



2.2.6 RMII MAC Mode

RMII MAC mode supports 10 or 100 Mbps full or half-duplex. RMII mac mode is typically used to connect an external PHY but can be used for other applications. In RMII MAC mode, REFCLK is an input and is expected to be 50 MHz for all data rates. Refer to Figure 11 for RMII MAC connection to an external PHY.

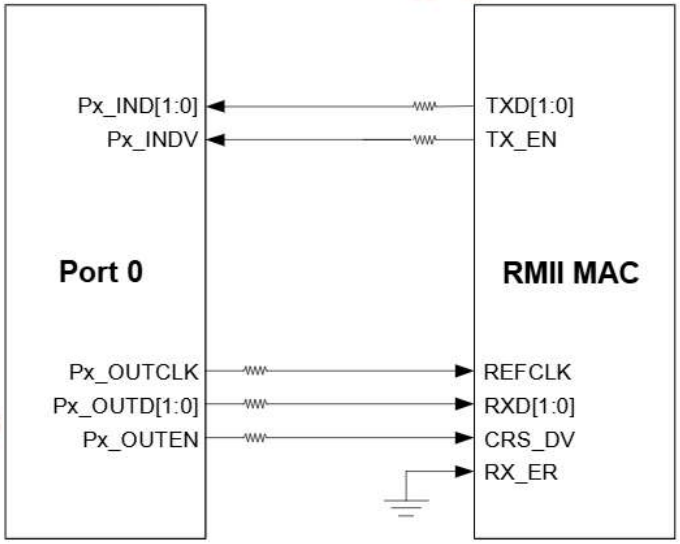
Figure 11: RMII MAC Interface Pins



2.2.7 RMII PHY Mode

In RMII PHY mode, REFCLK (P0_OUTCLK) is an output. OUTCLK is always 50 MHZ regardless of configured data interface speed. Figure 12 is an example of RMII PHY mode connections.

Figure 12: RMII PHY Interface



Note If COL and CRS are not used, they should be pulled- down with a 4.7 kohm resistor.

2.2.8 1000BASE-T PHY Interface

On 88E6390 and 88E6190 Ports 1-8 are integrated Gigabit PHY interfaces. On the 88E6290 Ports 1-8 are 100Base TX PHYs. All integrated PHYs support IEEE 802.3az Energy Efficient Ethernet standard. This allows the PHYs to enter a low power idle state when there is no traffic in either direction while still maintaining the link. The MAC inside the switch works the same way regardless of the external interface being used. Each PHY's Link, Speed, Duplex and Flow Control information is automatically communicated to the MAC. This information can be read on the Switch Port status register. The PHY core registers are not directly accessible via the SMI interface. All access to PHY registers must be performed indirectly via SMI_PHY_COMMAND and SMI_PHY_DATA registers. Other than customer specific PHY configuration there should be no reason for a CPU to continuously access internal PHY's registers.

2.2.9 SERDES modes

Port 9 and 10 have 1 SERDES lane each, P9_SMODE and P10_SMODE mode selects between 1000BASE-X/SERDES and 2.5G SERDES modes. Port 9 and 10 can be configured with register access to support other modes including SGMII MAC or PHY Modes.

2.2.10 SGMII MAC or PHY Mode

SGMII MAC mode is mode is used to connect a SERDES port to an external PHY. When the link state on the external PHY's media changes the new link state is communicated to switch MAC with in-band auto negotiation to the MAC.

SGMII PHY mode is typically used when the switch port is connected to a CPU or another switch.

SGMII mode supports 10/1000/1000 Mbps full or half-duplex. It uses the same 8B/10 encoding that 1000BASE-X uses. Lower speeds are supported by repeating the same symbol 10 times for 100 Mbps and 100 times to support 10 Mbps.

2.2.11 1000BASE-X

1000BASE-X is typically used to connect a switch port to an SFP fiber optics module. It can also be used to connect to another switch or CPU. 1000BASE-X supports auto negotiation bypass mode. This means the link can be established by receiving valid symbols. If the connected device only supports SGMII mode a link can be established by disabling auto negotiation on the connected device.

2.2.12 Port Status Registers

Each switch port has a status register that reports information about that port's PHY, SERDES or (x)MII interface. These registers can be used to check the current port configuration and link state. The C_MODE bits indicate the current configuration of the port. This is especially useful for auto media application to see which interface is currently internally connected to a given switch port. The port status register also indicates the speed duplex and if flow control is used.

2.2.13 PHY Polling Unit (PPU)

This device has an internal PHY polling unit. Clause 22 PHYs can be connected to MDC_PHY and MDIO_PHY pins. The PPU will automatically poll external PHYs using standard clause 22 defined PHY registers and update speed duplex and flow control in the MAC. By default the PPU is expecting the PHY connected to port 0 to be at external device address 0x0, Port 9 to be at external SMI address 0x9 and port 10 to be at SMI address 0x0A. After reset the PPU will attempt to read the registers on external PHYs. If PHY responds to SMI address 0x0 0x9 or 0xA, It will automatically set the PHY detect bit in port register 0 of the corresponding port. The PPU will then continuously monitor the link status of the PHY. If software does not want the PPU to perform this function it can clear the PHY detect bit which will cause the PPU stop polling that PHY at the end of the next poling cycle. The PPU polls PHY register 0,1,4,5,9,10 to determine the speed link duplex and flow control state of the PHY.

The SmiSetup function in the SMI_PHY_COMMAND register can be used to change the relationship between switch port and external PHY address. See functional spec for details.

Internal PHYs and External PHYs registers are accessed via the SMI_PHY_COMMAND register. This part has an internal SMI bus for accessing internal PHYs and an external SMI bus for accessing PHYs via the MDC_PHY and MDIO_PHY signals. This allows an external PHY to share the same SMI address with an external PHY without address conflicts.

Proprietary and clause 45 managed PHYs can be connected to MDC_PHY and MDIO_PHYs however the PPU cannot automatically manage them. In these usage cases the IMP or an external CPU must be used to communicate the state of the external PHY to the switch port using switch port register 1 and port register 2.

If NO_CPU is pulled low, the device is in CPU attached mode. The polling of external PHYs will not work until the NormalSMI bit in the scratch and misc. registers is cleared to 0. Refer to the release notes for the proper procedure for software to re-initialize the PPU. When the MDC_PHY and MDIO_PHY signals are enabled after reset IMP code or CPU must manually set the PHY detect bit.

2.3 General Purpose I/O (GPIO) Configuration

This device has 16 GPIO signals. GPIO[15:9] are dedicated GPIOs. GPIO[8:0] are available on Port 0 interface signals. Table indicates GPIO availability in all supported xMII modes.

Table 16: Port 0 GPIO Assignments

P5_MODE	xMII Setting	GPIO Available on Port 0	
000	Full-duplex MII PHY	GPIO [8:7]	When NO_CPU signal is pulled low at reset, These signals are defined as GPIO[8:7] When NO_CPU signal is pulled high at reset these signals are defied as MDC_PHY,MDIO_PHY. By clearing the NormalSMI bit (Global 2 Register 0x1A Index 0x2) the affect of the NO_CPU signal is inverted.
001	MII PHY	None Available	
010	MII MAC	None Available	
100	RMII PHY	GPIO [8:7], GPIO [6:5], GPIO [1]	
101	RMII MAC	GPIO [8:7], GPIO [6:5], GPIO [1]	
110	Disabled	GPIO[8:0]	
111	RGMII	GPIO [8;7]	When NO_CPU signal is pulled low at reset, These signals are defined as GPIO[8:7] When NO_CPU signal is pulled high at reset these signals are defied as MDC_PHY,MDIO_PHY. By clearing the NormalSMI bit (Global 2 Register 0x1A Index 0x2) the affect of the NO_CPU signal is inverted.

Once configured as a GPIO, the pin can be programmed to the following functions:

- P0_ENABLE
- General Purpose Input
- General Purpose Output
- Timing Application Interface (TAI)
  - PTP Trigger Output (PTP_TRIG)
  - PTP Event Request Input (PTP_EVREQ)
  - PTP External Clock Input (PTP_EXTCLK)
- Synchronous Ethernet Recovered Clock 0 Output (SE_RCLK0)
- Synchronous Ethernet Recovered Clock 1 Output (SE_RCLK1)
- 125 MHz Clock output
- Port Stall – can be used to stall the transmission of a specific port (or ports) as needed

These functions can be programmed through the Scratch and Misc Register at Switch Global 2, Offset 0x1A (see Functional Specification).

2.3.1 Configuring GPIO as a Port Enable Pin

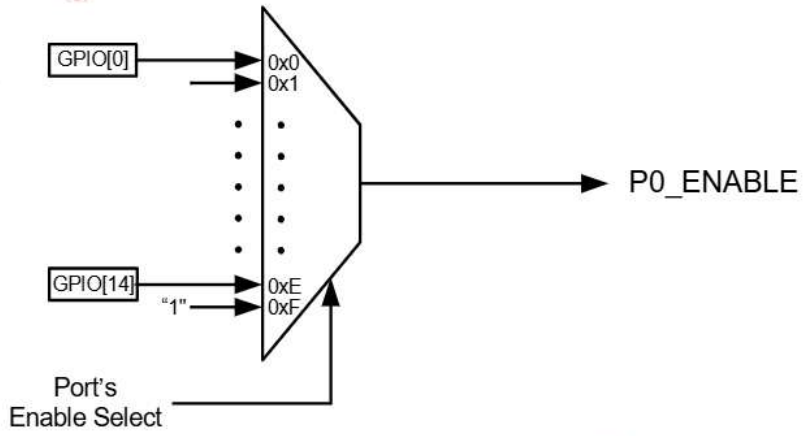
Each of the GPIO pins has the capability to be used as the P0_Enable pin for the xMII interfaces (Port 0) which can drive the link state of the port. When GPIO is used as P0_Enable the xMII output is tristated.

To use a GPIO as a Port Enable pin, the GPIO must first be configured as an input.

To select the specific GPIO to be used as an enable pin, program the xMII port's Enable Select register (Port Offset 0x1F, bits 15:12) to the number of the GPIO pin that will be used as the enable pin.

For example, setting the Enable Select to 0x0 selects GPIO 0, 0x1 selects GPIO 1, etc. Setting the bits to 0xF connects the enable function to a logic high, enabling the interface. Refer to Figure 13 for a configuration diagram. When the port does not have any GPIO selected the input state to Px_Enable is 1 so the link will be up if the PHY Detect bit in port register 0=0. When the PHY detect bit is 1 the link state will be driven by the PPU results.

Figure 13: GPIO Enable Example



2.4 LED Interface

The device uses a matrix LED interface allowing each PHY port to have up to two LEDs. The cathode of each LED is connected to a single row signal (Rx_LED). The anode of each LED is connected to a single column signal (Cx_LED). The physical LEDs on the device pins are organized as 5 rows with 4 columns. Table 17 shows the port to physical mapping.

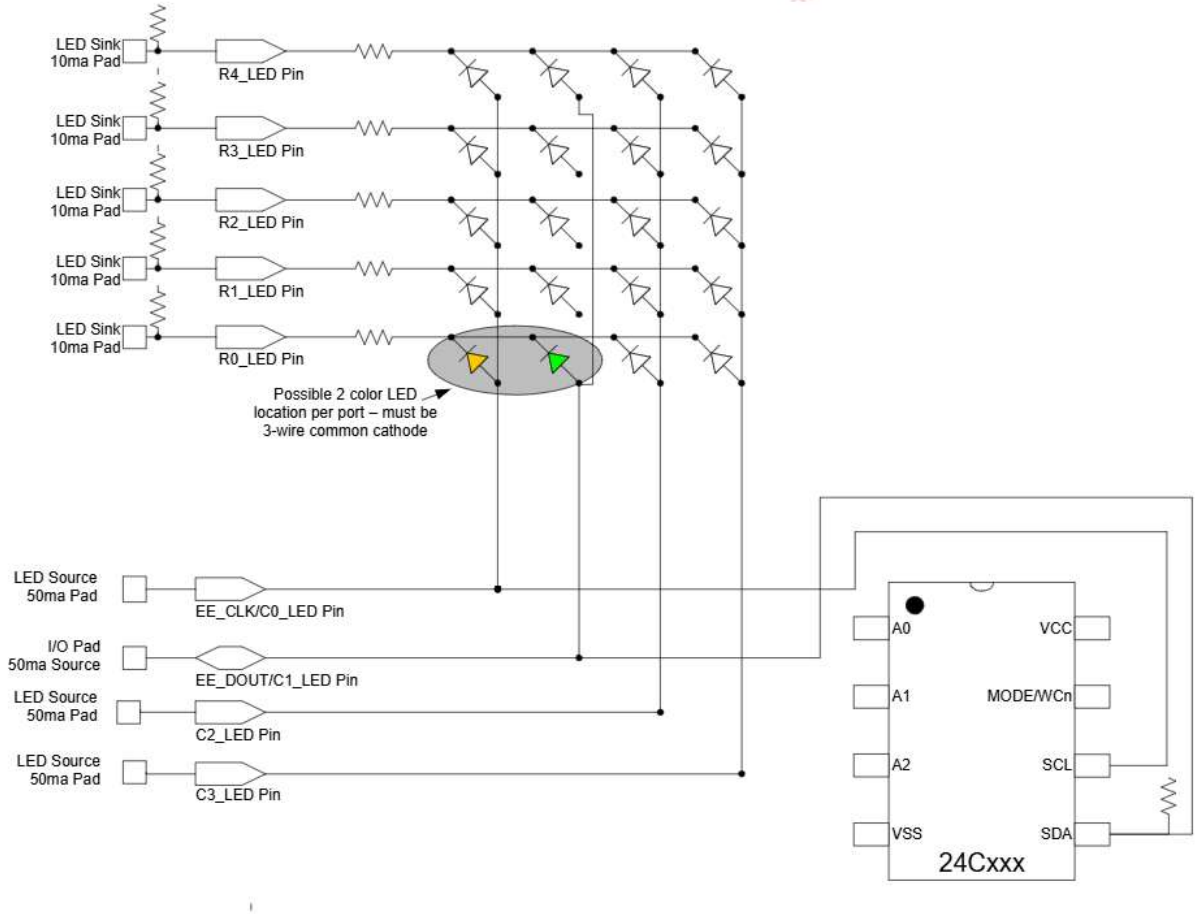
Table 17: LED Mapping

	C0_LED	C1_LED	C2_LED	C3_LED
R0_LED	Port 1, LED 0	Port 1, LED 1	Port 2, LED 0	Port 2, LED 1
R1_LED	Port 3, LED 0	Port 3, LED 1	Port 4, LED 0	Port 4, LED 1
R2_LED	Port 5, LED 0	Port 5, LED 1	Port 6, LED 0	Port 6, LED 1
R3_LED	Port 7, LED 0	Port 7, LED 1	Port 8, LED 0	Port 8, LED 1
R4_LED	Port 9, LED 0	Port 9, LED 1	Port 10, LED 0	Port 10, LED 1

The column signals (Cx_LED) are also shared with the EEPROM interface, and the architecture allows for the LEDs and EEPROM to operate at the same by time multiplexing the bus into 6 time cycles (C0_LED, C1_LED, C2_LED, C3_LED, and EEPROM). This prevents EEPROM access from interfering with LED operation and vice versa.

Refer to Figure 14 for EEPROM LED design.

Figure 14: LEDs plus 2 wire EEPROM



The EEPROM type can be 24C32-24C512

2.4.1 LED Options

Each port supports up to two LEDs that can be configured individually to support many different options. Please note some functions are not supported on all LEDs.

Port 1-8 LED0 can be configured in one of the following modes:

- Link/Act/Speed by Blink Rate3 (off = no link, on = link, blink = activity,
- blink speed = link speed4)
- 100/Gb Link/Act (off = no link, on = 100 or Gb link, blink = activity)
- Gb Link/Act (off = no link, on = Gb link, blink = activity)
- Link/Act (off = no link, on = link, blink = activity)
- Duplex/Collision (off = half-duplex, on = full-duplex, blink = col)
- 10/Gb Link/Act (off = no link, on = 10 or Gb link, blink = activity)
- Link (off = no link, on = link)
- 10 Link (off = no link, on = 10 link)
- 10 Link/Act (off = no link, on = 10 link, blink = activity)
- 100/Gb Link (off = no link, on = 100 or Gb link)
- PTP Act (blink on = PTP activity) - not valid on 88E6190 & 6190X
- Force Blink
- Force Off
- Force On

Port 1-8 LED1 can be configured in one of the following modes:

- 10/100 Link/Act (off = no link, on = 10 or 100 link, blink = activity)
- 10/100 Link/Act (off = no link, on = 10 or 100 link, blink = activity)
- Gb Link (off = no link, on = Gb link)
- Link/Act (off = no link, on = link, blink = activity)
- 10/Gb Link/Act (off = no link, on = 10 or Gb link, blink = activity)
- 10/Gb Link (off = no link, on = 10 or Gb link)
- Gb Link/100 Blink (off = no link or 10 Link, blink = 100 Link, on = Gb
- Link)
- 100 Link (off = no link, on = 100 link)
- 100 Link/Act (off = no link, on = 100 link, blink = activity)
- 10/100 Link (off = no link, on = 10 or 100 link)
- PTP Act (blink on = PTP activity) - not valid on 88E6190 & 6190X
- Force Blink
- Force Off
- Force On

The LED select configuration signal determines the value of port register 0x16 Index 0x0 Table 18,Table 19 and Table 20 indicates the default behavior of the LEDs for each supported hardware configuration. The LED configuration can be changed at any time with register access.

Table 18: Port 1-8 Hardware Reset LED configuration

LED_SEL	LED Mode (Port 1-8 register 0x16 Index 0x0)	LED 0	LED 1
1	0x2	Gb Link/Act: off = No link on = Gb link blink = Activity	10/100 Link/Act off = No link on = 10/100 link, blink = Activity)
0	0x3	Link/Act: off = No link on = Link blink = Activity	0x3 = Gb Link (off = no link, on = Gb link)

Table 19: Port 9 Hardware Reset LED configuration

LED_SEL	LED Mode (Port 9 Register 0x16 Index 0x0)	LED 0	LED 1
1	0x2	Port 0 Link/Activity	Port 10 Link Activity
0	0x3	Port 9 Link/Activity	Combined Link/Activity for ports 1-8

Table 20: Port 10 Hardware Reset LED configuration

LED_SEL	LED Mode (Port register 0x16)	LED 0	LED 1
1	0x2	PTP Activity	Port 9 Link/Activity
0	0x3	Port 10 Link Activity	Port Link/Activity

2.4.2 Special LEDs

Special LEDs are used to display the Link/Activity status on a group of ports.This device supports 4 Special LED groups. A special LED group can be assigned to LED 0 or LED 1 on any port. A typical applicator where Special LEDs are used is all the LAN ports are combined into a single LED. A special LED group can be assigned to more than one LED. See LED control registers in the Functional specification.

2.5 Connection of external PHYs

Port 0, Port 9 and Port 10 can be connected to external PHYs. The PHY polling unit can be used to poll any standard 802.3 Clause 22 compliant PHY. The PHY polling unit communicates the link, speed, duplex, and flow control state of the PHY. After reset the PPU will poll SMI address 0x00 for port 0, 0x09 for port 9 and 0x0A for port 10. With register access, the association between external SMI address and switch port can be changed by using the SmiSetup operation in Global 2. An external PHY's SMI addresses can be any PHY address between 0 and 0x1F.

2.5.1 Connection to 1000BASE-T PHY

Figure 15 represents a typical connection to an external 1000BASE- T PHY using SGMII on ports 9 and 10. Unused SERES lanes can be used in auto media detect mode with ports 2-7. Depending on trace length, if multiple PHYs are connected, a buffer on MDC_PHY is advisable.

Figure 15: Typical SGMII connection to external PHY connections

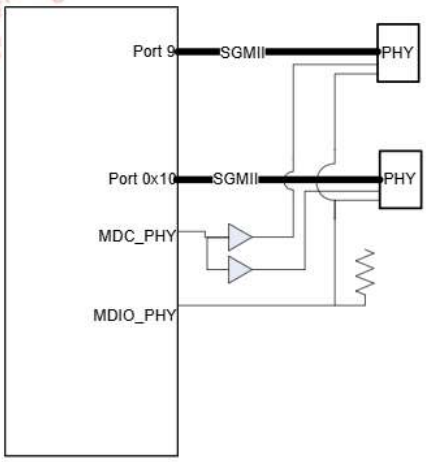
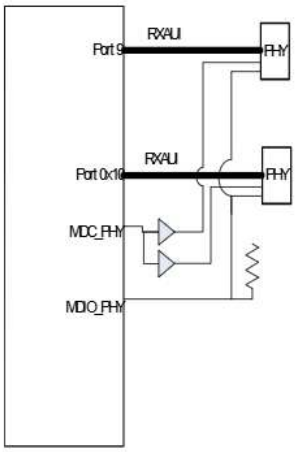


Figure 16: Typical external 10G PHY connection



3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 21: Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD(3.3)}$	Power Supply Voltage on any 3.3V signal with respect to VSS	-0.5	3.3	+3.6	V
$V_{DD(2.5)}$	Power Supply Voltage on any 2.5V signal with respect to VSS	-0.5	2.5	+3.6 or $V_{DD(3.3)}$ +0.5[1] whichever is less	V
$V_{DD(1.8)}$	Power Supply Voltage on any 1.8V supply with respect to VSS	-0.5	1.8	+3.6 or $V_{DD(2.5)}$ +0.5[2] whichever is less	V
$V_{DD(1.5)}$	Power Supply Voltage on any 1.5V supply with respect to VSS	-0.5	1.5	+3.6 or $V_{DD(1.8)}$ +0.5[3] whichever is less	V
$V_{DD(1.1)}$	Power Supply Voltage on any 1.05V supply with respect to VSS	-0.5	1.1 1.1(I-grade)	+3.6 or $V_{DD(1.5)}$ +0.5[4] whichever is less	V
V_{PIN}	Voltage applied to any input pin with respect to VSS	-0.5		+3.6 or V_{DDO_PIN}[5] +0.5[6] whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[7]	°C

1. VDD(2.5) must never be more than 0.5V greater than VDD(3.3) or damage will result. Power must be applied to VDD(3.3) before or at the same time as VDD(2.5).
2. VDD(1.8) must never be more than 0.5V greater than VDD(2.5) or damage will result. Power must be applied to VDD(2.5) before or at the same time as VDD(1.8).
3. VDD(1.5) must never be more than 0.5V greater than VDD(1.8) or damage will result. Power must be applied to VDD(1.8) before or at the same time as VDD(1.5).
4. VDD(1.1) must never be more than 0.5V greater than VDD(1.5) or damage will result. Power must be applied to VDD(1.5) before or at the same time as VDD(1.05).
5. The VDDO pad ring has separate I/O power supply options. Therefore, the voltage applied to a group of I/O pins must follow what is defined in Section 1.
6. VPIN must never be more than 0.5V greater than VDDO or damage will result.
7. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

3.1.1 Power Supply Sequencing

Power supply voltage on any pin must never be more than 0.5V greater than the next highest voltage pin, or damage will result. Power must be applied to the higher voltage pin before or at the same time as power is applied to the pins with the next lower voltage.

3.2 Recommended Operating Conditions

Table 22: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	3.3V power supply	For any 3.3V supply pin[1]	3.135	3.3	3.465	V
$V_{DD(2.5)}$	2.5V power supply	For any 2.5V supply pin[2]	2.375	2.5	2.625	V
$V_{DD(1.8)}$	1.8V power supply	For any 1.8V supply pin	1.710	1.8	1.890	V
$V_{DD(1.5)}$	1.5V power supply	For any 1.5V supply pin	1.425	1.5	1.575	V
$V_{DD(1.05)Commercial}$	1.05V power supply	For any 1.05V supply pin	0.998	1.05	1.155	V
$V_{DD(1.10)Industrial}$	1.10V Power supply	For any 1.10V supply	1.045	1.1	1.155	V
T_A	Ambient operating temperature[3]	Commercial parts	0		70	°C
		Industrial parts[4]	-40		85	°C
T_J	Maximum junction temperature				125[2]	°C
RSET	Internal bias reference	External resistor value required to be placed between RSET and VSS pins	4950	5000	5050	Ω

1. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
2. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
3. The important parameter is maximum junction temperature. As long as the maximum junction temperature is not exceeded, the device can be operated at any ambient temperature. Refer to White Paper on "TJ Thermal Calculations" for more information.
4. Industrial part numbers have an "I" following the commercial part numbers. For details see Section 5, Part Order Numbering/Package Marking, on page 94.

3.3 Thermal Conditions

3.3.1 Thermal Conditions for the 88E6390/88E6190/88E6290 device 144-pin QFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient of the 144-Pin QFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		23.6		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		21.2		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		20.1		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		19.3		°C/W
Ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 144-Pin QFP package $\Psi_{JT} = (T_J - T_{TOP})/P$. T_{TOP} = Temperature on the top center of the package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.24		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.35		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.47		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		0.53		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 144-Pin QFP package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		8.5		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 144-Pin QFP package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		14.6		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

3.4 Current Consumption

Table 23: 88E6390/88E6190/88E6290 Device Current Consumption

Pins	Parameter	Condition	Min	Typ	Max	Units
Px_AVDD33	3.3V power to analog core for Gig PHY interfaces	All ports active (Port 1 - Port 8 at 1000 Mbps) Not applicable to 88E6290		418		mA
		All ports active (Port 1 - Port 8 at 100 Mbps)		114		mA
		All ports active (Port 1 - Port 8 at 10 Mbps)		213		mA
		EEE disabled, all ports idle (Port 1 - Port 8 linked at 1000 Mbps but idle)		418		mA
		EEE disabled, all ports idle (Port 1 - Port 8 linked at 100 Mbps but idle)		113		mA
		EEE disabled, all ports idle (Port 1 - Port 8 linked at 10 Mbps but idle)		117		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		12		mA
		EEE enabled, all ports idle (linked at 100 Mbps)		12		mA
		EEE disabled 1 port linked at 1000 Mbps full traffic, all other GPHY's powered down		65		mA
		1 port linked at 100 Mbps full traffic, all other GPHY's powered down		26		mA
		1 port linked at 10 Mbps full traffic, all other GPHY's powered down		38		mA
		1 port linked at 1000 Mbps, idle		65		mA
		1 port linked at 100 Mbps, idle		26		mA
		1 port linked at 10 Mbps, idle		26		mA
		1 port Gig EEE, all other GPHY's powered down		18		mA
		1 port 100 EEE, all other GPHY's powered down		13		mA
		No link on any port		12		mA
		Reset		12		mA

Table 23: 88E6390/88E6190/88E6290 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
Px_AVDD15	1.5V power to analog core for Gig PHY interfaces	All ports active (Port 1 - Port 8 at 1000 Mbps)		273		mA
		All ports active (Port 1 - Port 8 at 100 Mbps)		141		mA
		All ports active (Port 1 - Port 8 at 10 Mbps)		110		mA
		EEE disabled, all ports idle (Port 1 - Port 8 linked at 1000 Mbps but idle)		270		mA
		EEE disabled, all ports idle (Port 1 - Port 8 linked at 100 Mbps but idle)		138		mA
		EEE disabled, all ports idle (Port 1 - Port 8 linked at 10 Mbps but idle)		107		mA
		EEE enabled, all ports idle (linked at 1000 Mbps)		135		mA
		EEE enabled, all ports idle (linked at 100 Mbps)		105		mA
		1 port linked at 1000 Mbps, full traffic		40		mA
		1 port linked at 100 Mbps, full traffic		23		mA
		1 port linked at 10 Mbps, full Traffic		19		mA
		1 port linked at 1000 Mbps, idle		40		mA
		1 port linked at 100 Mbps, idle		23		mA
		1 port linked at 10Mbps, idle		19		mA
		1 port 1000 Mbps EEE idle		25		mA
		1 port 100 Mbps EEE idle		18		mA
		No link on any port		88		mA
		Reset		27		mA
AVDD15_ XTAL	1.5V power to power the on-chip XTAL.	--		6		mA

Table 23: 88E6390/88E6190/88E6290 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
EE_VDDO	3.3V to EEPROM and LED pins.	All ports active at max speed		34		mA
		All ports active at 100 Mbps		19		mA
		All ports active at 10 Mbps		19		mA
		Reset		39		mA
		No link on any port		4		mA
P0_VDDO	2.5V for Port 0's RGMII/MII/RMII I/O pins.	Port active at 1000 Mbps		33		mA
		Port active at 100 Mbps		9		mA
		Port active at 10 Mbps		5		mA
		Reset		3		mA
		Link down		5		mA
		Interface disabled (P0_MODE = 0x6)		4		mA
	1.8V for Port 0's RGMII/MII/RMII I/O pins.	Port active at 1000 Mbps		23		mA
		Port active at 100 Mbps		6		mA
		Port active at 10 Mbps		6		mA
		Reset		2		mA
		Link Down		3		mA
		Interface disabled (P0_MODE = 0x6)		3		mA
GPIO_VDDO	2.5V for GPIO pins. See GPIO_VDDO pin definition in Table 8 for details as to which pins are powered by GPIO_VDDO.	Reset		2		mA
	1.8V for GPIO pins. See GPIO_VDDO pin definition in Table 8 for details as to which pins are powered by GPIO_VDDO.	Reset		1		mA
P9_AVDD15 P10_AVDD15	1.5V power to SERDES	Port 9 and Port 10 2500BASE-X		140		mA
		Port 9 and Port 10 1000BASE-X		80		mA
		All Lanes powered down		7		mA
		Reset		7		mA

Table 23: 88E6390/88E6190/88E6290 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
VDD_ CORE	1.1V power to digital core	All ports active at max speed, P9 and P10 2500BASE-X		1065		mA
		All ports active at 100 Mbps P9 and P10 2500BASE-X		552		mA
		All ports active at 10 Mbps, P9 and P10 2500BASE-X		524		mA
		EEE disabled, all ports idle and linked at 1000 Mbps, P9 and P10 1000BASE-X		181		mA
		EEE disabled, all ports idle and linked at 100 Mbps, P9 and P10 1000BASE-X		135		mA
		EEE disabled, all ports idle and linked at 10 Mbps, P9 and P10 1000BASE-X		129		mA
		No link on any port		145		mA
		EEE enabled (All ports idle @ 1G, P9 and P10 1000BASE-X)		175		mA
		Link on one port 1000 Mbps (RGMII disabled, P2-8 Powered down, P9, P10 EEE disabled, All SERDES Powered down)		138		mA
		Link on one port 100 Mbps (RGMII disabled, P2-8 Powered down, P9, P10 EEE disabled, All SERDES Powered down)		90		mA
		Link on one port 10 Mbps (RGMII disabled, P2-8 Powered down, P9, P10 EEE disabled, All SERDES Powered down)		86		mA
		One port linked 1000Mbps EEE (RGMII disabled, P2-8 Powered down, P9, P10 EEE disabled, All SERDES Powered down)		90		mA
		All ports powered down (RGMII disabled, P1-8 Powered down, P9, P10 EEE disabled, All SERDES Powered down)		82		mA
		Reset		41		mA

3.5 DC Electrical Characteristics

3.5.1 Digital Operating Conditions

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 24: Digital Operating Conditions

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VDDO	3.3V power.	See EE_VDDO pin definition in Table 10 for details.		3.135	3.3	3.465	V
	2.5V/1.8V power.	See P0_VDDO and GPIO_VDDO pin definitions in Table 10 for details.		2.375	2.5	2.625	V
				1.71	1.8	1.89	V
V_{IH}	High level input voltage	XTAL_IN, SE_SCLK	AVDD15	1.4		1.99	V
		EE_VDDO	VDDO = 3.135V	VDDO*70%		VDDO+0.4	V
		P0_VDDO GPIO_VDDO	VDDO = 2.375V				V
			VDDO = 1.710V				V
V_{IL}	Low level input voltage	XTAL_IN, SE_SCLK	AVDD15	-0.3		0.54	V
		EE_VDDO	VDDO = 3.135V	-0.4		VDDO*30%	V
		P0_VDDO GPIO_VDDO	VDDO = 2.375V				V
			VDDO = 1.710V				V
V_{OH}	High level output voltage	LED pins	I_{OH} = -7 mA	VDDO - 0.4			V
		All others (except INTn [1])	I_{OH} = -4 mA	VDDO - 0.4			V
		Others @ 1.8V	I_{OH} = -2 mA	VDDO - 0.2			V
V_{OL}	Low level output voltage	INTn and LED pins	I_{OL}= 7 mA			0.4	V
		All others	I_{OL}= 4 mA			0.4	V
		Others 1.8V	I_{OL}= 2 mA			0.2	V
I_{ILK}	Input leakage current	With pull-up resistor	$0<V_{IN}<V_{DDO}$			+ 10 - 60	µA
		With pull-down resistor	$0<V_{IN}<V_{DDO}$			+ 60 - 10	µA
		Others	$0<V_{IN}<V_{DDO}$			+ 10 - 10	µA
C_{IN}	Input capacitance	XTAL_IN, SE_SCLK			5		pF
		All others				5	pF

1. The INTn is an active low, open drain pin. See INTn description in the Signal Description.

3.5.2 SGMII Interface

SGMII specification is a de-facto standard proposed by Cisco. It is available at the Cisco website ftp://ftp-eng.cisco/smii/sgmii.pdf. It uses a modified LVDS specification based on the IEEE standard 1596.3. Refer to that standard for the exact definition of the terminology used in the following table. The device adds flexibility by allowing programmable output voltage swing and supply voltage option.

3.5.2.1 Transmitter DC Characteristics

Symbol	Parameter[1]	Min	Typ	Max	Units
V_{OH}	Output Voltage High			1400	mV
V_{OL}	Output Voltage Low	700			mV
V_{RING}	Output Ringing			10	%
$\|V_{OD}\|^2$	Output Voltage Swing (differential, peak)	Programmable - see Table 25.			mV peak
V_{OS}	Output Offset Voltage (also called Common mode voltage)	Variable - see 3.5.2.2 for details.			mV
R_O	Output Impedance (single-ended) (50 ohm termination)	40		60	Ωs
Delta R_O	Mismatch in a pair			10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1			25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1			25	mV
I_{S+}, I_{S-}	Output current on short to VSS			40	mA
I_{S+-}	Output current when S_OUT+ and S_OUT- are shorted			12	mA
I_{X+}, I_{X-}	Power off leakage current			10	mA

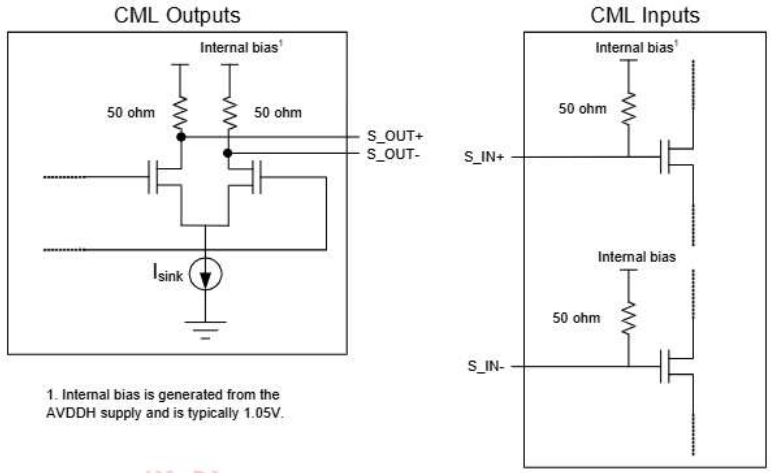
1. Parameters are measured with outputs AC connected with 100 ohm differential load.
2. Output amplitude is programmable by writing to Register 26_1.2:0.

Table 25: Programming SGMII Output Amplitude

Register 26_1 Bits	Field	Description
2:0	SGMII/Fiber Output Amplitude[1]	Differential voltage peak measured. Note that internal bias minus the differential peak voltage must be greater than 700 mV. 000 = 14 mV 001 = 112 mV 010 = 210 mV 011 = 308 mV 100 = 406 mV 101 = 504 mV 110 = 602 mV 111 = 700 mV

1. Cisco SGMII specification limits are |VOD| = 150 mV - 400 mV peak differential.

Figure 17: CML I/Os



1. Internal bias is generated from the AVDDH supply and is typically 1.05V.

3.5.2.2 Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII/Fiber interface connections. These are:

- DC connection to an LVDS receiver
- AC connection to an LVDS receiver
- DC connection to an CML receiver
- AC connection to an CML receiver

If AC coupling or DC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- Internal bias. See Figure 17 for details. (If AVDD18 is used to generate the internal bias, the internal bias value will typically be 1.05V.)
- The output voltage swing is programmed by Register 26_1.2:0 (see Table 25).
- Voffset (i.e., common mode voltage) = internal bias - single-ended peak-peak voltage swing. See Figure 18 for details.

If DC coupling is used with a CML receiver, then the DC levels will be determined by a combination of the MACs output structure and the input structure shown in the CML Inputs diagram in Figure 19. Assuming the same MAC CML voltage levels and structure, the common mode output levels will be determined by:

- Voffset (i.e., common mode voltage) = internal bias - (single-ended peak-peak voltage swing/2). See Figure 19 for details.
- If DC coupling is used, the output voltage DC levels are determined by the AC coupling considerations above, plus the I/O buffer structure of the MAC.

Figure 18: AC connections (CML or LVDS receiver) or DC connection LVDS receiver

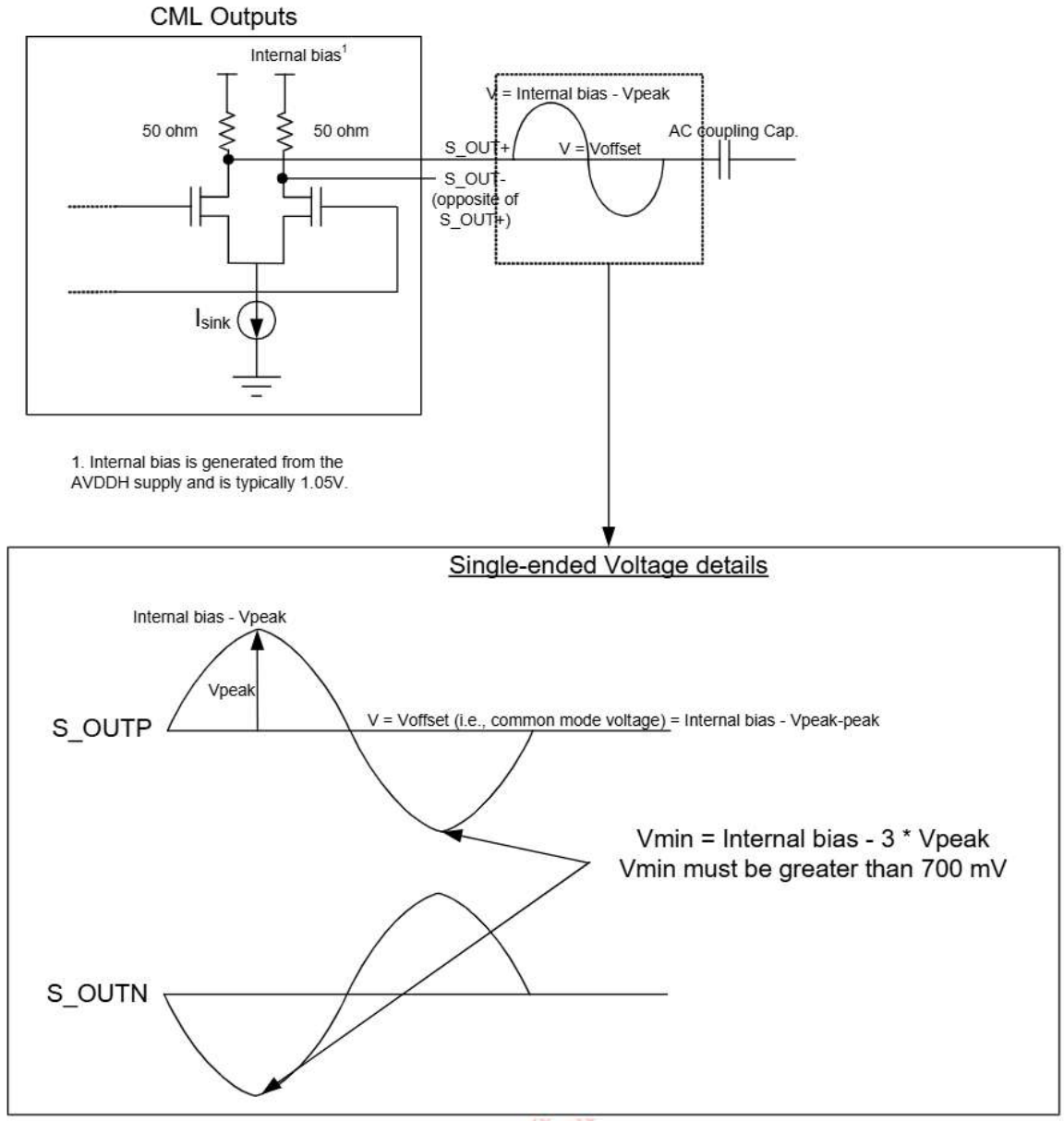
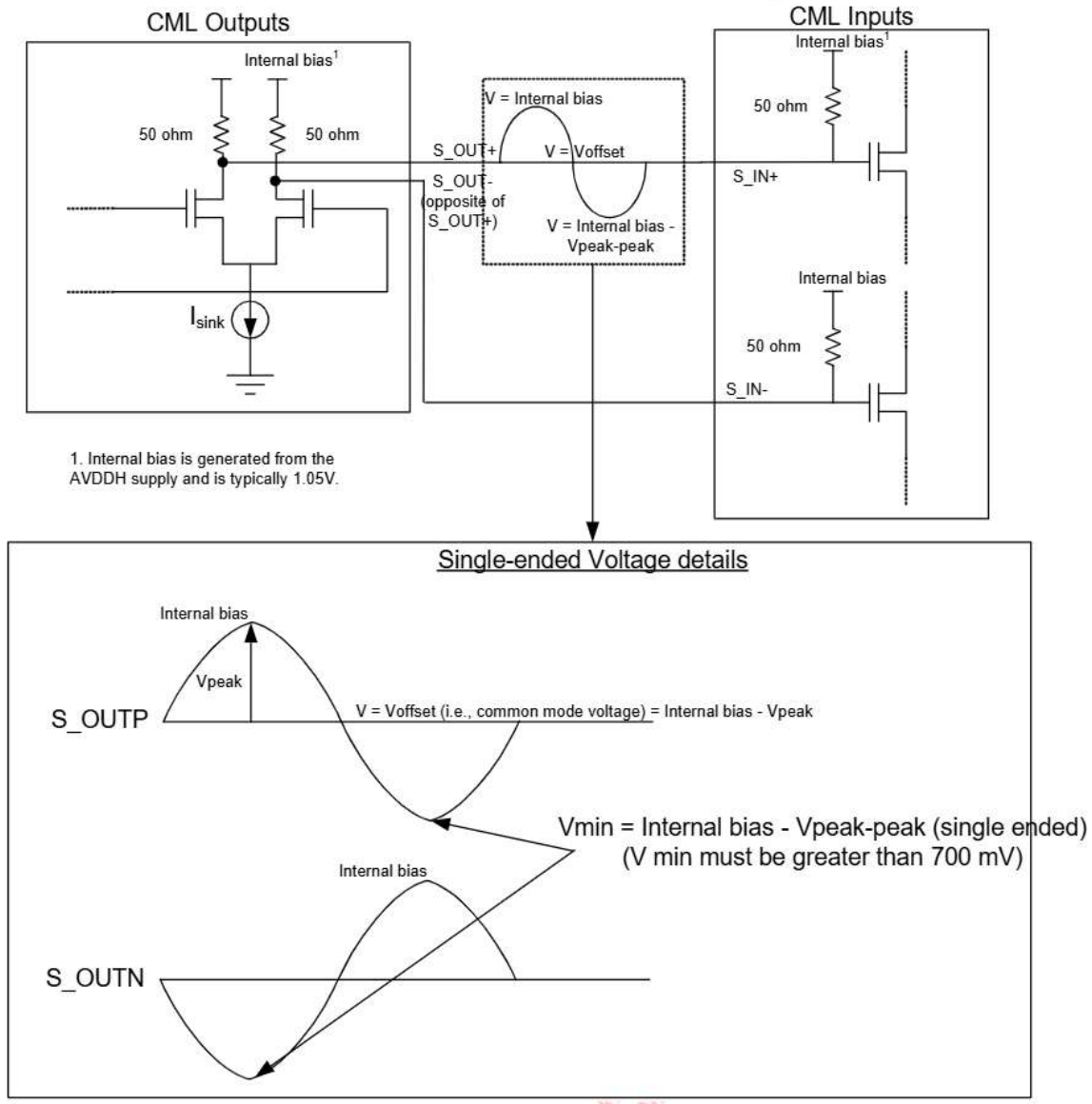


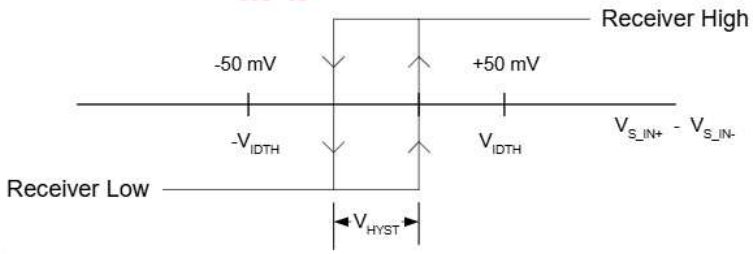
Figure 19: DC connection to a CML receiver



3.5.2.3 Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_I	Input Voltage range a or b	675		1725	mV
V_{IDTH}	Input Differential Threshold	-50		+50	mV
V_{HYST}	Input Differential Hysteresis	25			mV
R_{IN}	Receiver 100 Ω Differential Input Impedance	80		120	Ω

Figure 20: Input Differential Hysteresis



3.6 AC Electrical Specifications

3.6.1 Reset and Configuration Timing

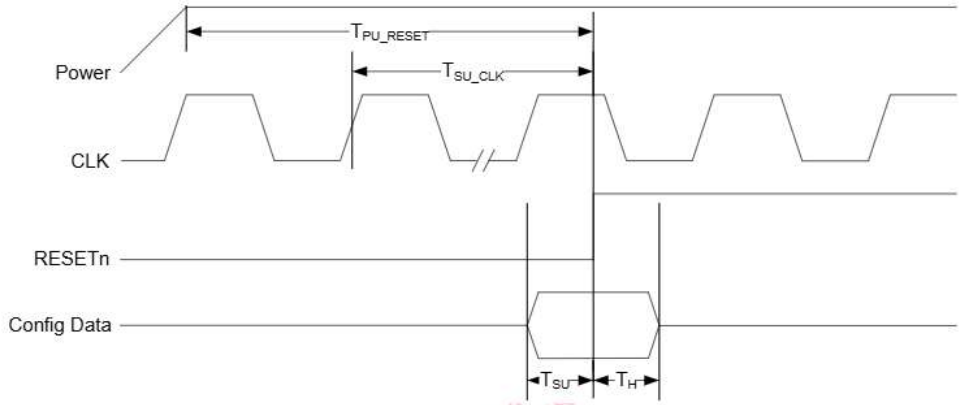
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 26: Reset and Configuration

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted or RESETn assertion time	At power up or sub-sequent resets after power up	10			ms
T_{SU_CLK}	Number of valid REFCLK cycles prior to RESETn de-asserted		10			Clks
T_{SU}	Configuration data valid prior to RESETn de-asserted[1]		200			ns
T_{HD}	Config data valid after RESETn de-asserted		0			ns

1. When RESETn is low all configuration pins become inputs, and the value seen on these pins is latched on the rising edge of RESETn. All configuration pins that become outputs during normal operation will remain tri-stated for 40 ns after the rising edge of RESETn.

Figure 21: Reset and Configuration Timing



3.6.2 Clock Timing

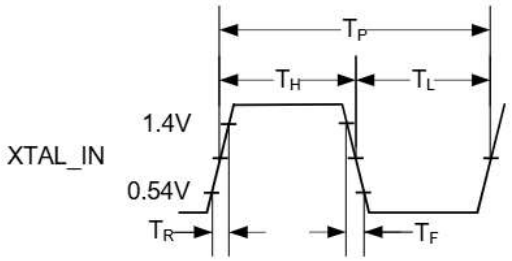
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 27: IEEE DC Transceiver Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P[1]	XTAL_IN period		40 -50 ppm	40	40 +50 ppm	ns
T_H	XTAL_IN high time		13	20	27	ns
T_L	XTAL_IN low time		13	20	27	ns
T_R	XTAL_IN rise				3	ns
T_F	XTAL_IN fall				3	ns
$T_{J\_XTAL\_IN}$	XTAL_IN total jitter[2]				200	ps[3]

1. If the crystal option is used, ensure that the frequency is 25.000 MHz ± 50 ppm.
2. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
3. Broadband peak-peak = 200 ps, Broadband rms = 3 ps, 12 kHz to 20 MHz rms = 1 ps.

Figure 22: Oscillator Clock Timing



3.7 MII Timing

3.7.1 MII PHY Mode Receive Timing - 100 Mbps

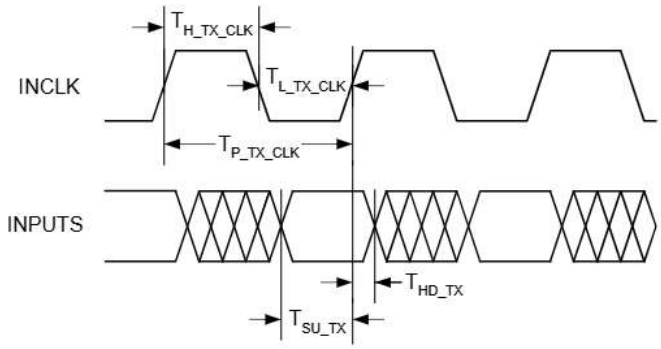
In PHY mode, the P[x]_INCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 28: MII PHY Mode Receive Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$[1]	P[x]_INCLK period	10BASE mode		400		ns
		100BASE mode		40		ns
$T_{H\_TX\_CLK}$	P[x]_INCLK high	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
$T_{L\_TX\_CLK}$	P[x]_INCLK low	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
T_{SU_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high.		15			ns
T_{HD_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high.		0			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 23: MII PHY Mode Receive Timing



NOTE: INCLK is the clock used to clock the input data. It is an output in this mode.

3.7.2 MII PHY Mode Transmit Timing - 100 Mbps

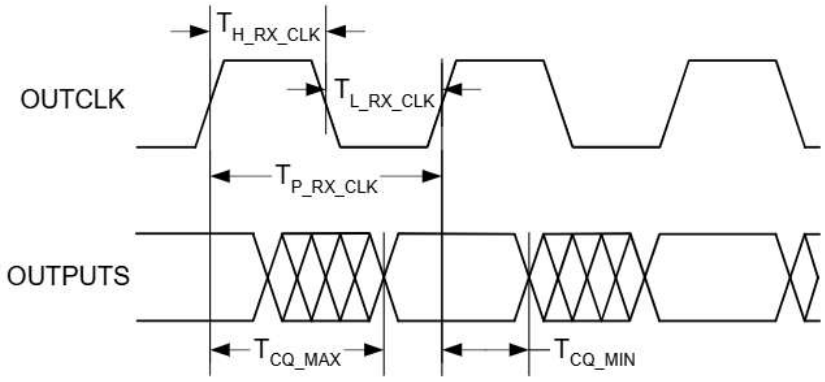
In PHY mode, the P[x]_OUTCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 29: MII PHY Mode Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	10BASE mode		400		ns
		100BASE mode		40		ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid				25	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[3:0], P[x]_OUTEN) invalid		10			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 24: MII PHY Mode Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an output in this mode.

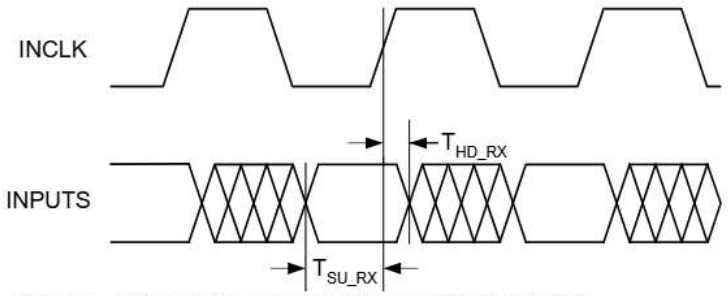
3.7.3 MII MAC Mode Receive Timing

In MAC mode, the P[x]_INCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 30: MII Receive Timing - MAC Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high	With 10 pF load	10			ns
T_{HD_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high	With 10 pF load	10			ns

Figure 25: MII MAC Mode Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an input in this mode.

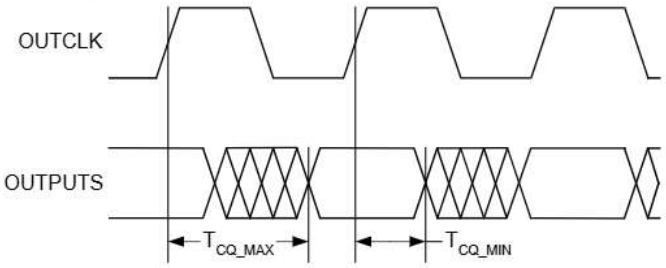
3.7.4 MII MAC Mode Transmit Timing

In MAC mode, the P[x]_OUTCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 31: MII MAC Mode Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid	With 10 pF load			25	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) invalid	With 10 pF load	0			ns

Figure 26: MII MAC Mode Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an input in this mode.

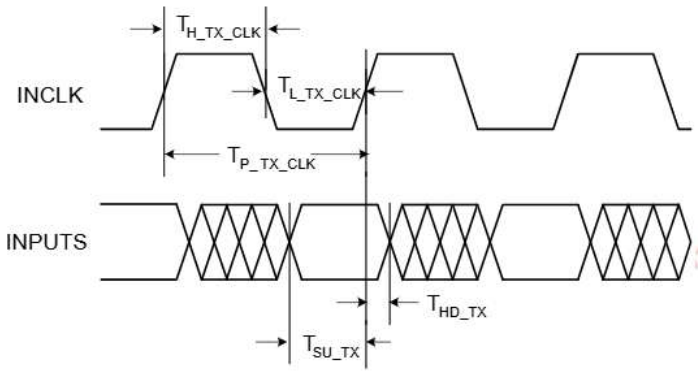
3.7.5 TMII PHY Mode Receive Timing - 200 Mbps

In PHY mode, the P[x]_INCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 32: TMII PHY Mode Receive Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$	P[x]_INCLK period	200BASE mode		20		ns
$T_{H\_TX\_CLK}$	P[x]_INCLK high	200BASE mode	8	10	12	ns
$T_{L\_TX\_CLK}$	P[x]_INCLK low	200BASE mode	8	10	12	ns
T_{SU_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high.		5			ns
T_{HD_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high.		3			ns

Figure 27: TMII PHY Mode Receive Timing - 200 Mbps



NOTE: INCLK is the clock used to clock the input data. It is an output in this mode.

3.7.6 TMII PHY Mode Transmit Timing - 200 Mbps

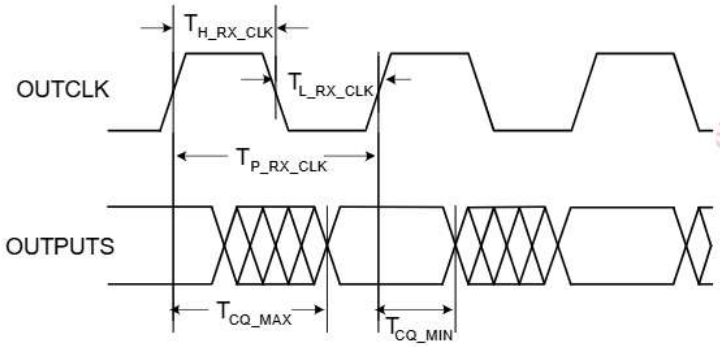
In PHY mode, the P[x]_OUTCLK pins are outputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified).

Table 33: TMII PHY Mode Transmit Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	200BASE mode		20		ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	200BASE mode	8	10	12	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	200BASE mode	8	10	12	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid				15	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[3:0], P[x]_OUTEN) invalid		2			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 28: TMII PHY Mode Transmit Timing - 200 Mbps



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

3.7.7 TMII MAC Mode Clock Timing - 200 Mbps

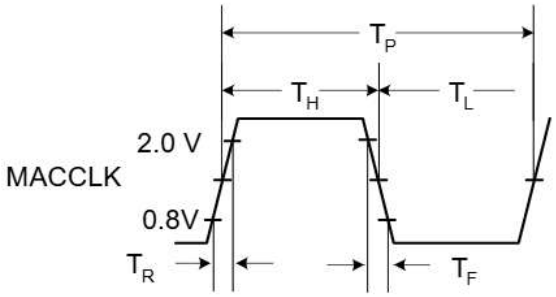
In MAC mode, INCLK and OUTCLK are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified).

Table 34: TMII MAC Mode Clock Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P[1]	MACCLK_IN period		0	20	20 +50 ppm	ns
T_H	MACCLK_IN high time		8			ns
T_L	MACCLK_IN low time		8			ns
T_R	MACCLK_IN rise				3	ns
T_F	MACCLK_IN fall				3	ns

1. DC to 25 MHz

Figure 29: TMII MAC Clock Timing - 200 Mbps



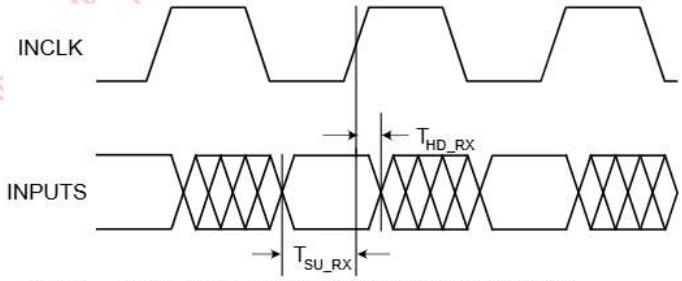
3.7.8 TMII MAC Mode Receive Timing - 200 Mbps

In MAC mode, the P[x]_INCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified).

Table 35: TMII MAC Mode Receive Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high	With 10 pF load	5			ns
T_{HD_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high	With 10 pF load	2			ns

Figure 30: TMII MAC Mode Receive Timing - 200 Mbps



NOTE: INCLK is the clock used to clock the input data. It is an input in this mode.

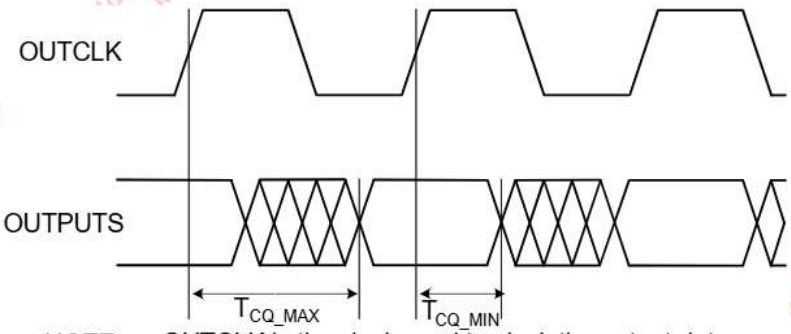
3.7.9 TMII MAC Mode Transmit Timing - 200 Mbps

In MAC mode, the P[x]_OUTCLK pins are inputs.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified).

Table 36: TMII MAC Transmit Timing - 200 Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTDV valid	With 10 pF load			15	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTDV invalid	With 10pF load	0			ns

Figure 31: TMII MAC Mode Transmit Timing - 200 Mbps



NOTE: OUTCLK is the clock used to clock the output data. It is an input in this mode.

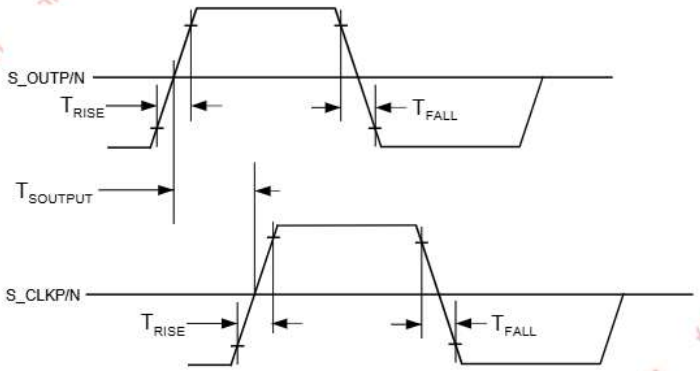
3.8 SGMII Timing

3.8.1 SGMII Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{FALL}	V_{OD} Fall time (20% - 80%)	100		200	ps
T_{RISE}	V_{OD} Rise time (20% - 80%)	100		200	ps
CLOCK	Clock signal duty cycle @ 625 MHz	48		52	%
T_{SKEW1}[1]	Skew between two members of a differential pair			20	ps
$T_{SOUTPUT}$[2]	SERDES output to RxClk_P/N	360	400	440	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14*rms Random)		127		ps

1. Skew measured at 50% of the transition.
2. Measured at 50% of the transition.

Figure 32: Serial Interface Rise and Fall Times



3.8.2 SGMII Input AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14*rms Random)			599	ps

3.9 RGMII Timing

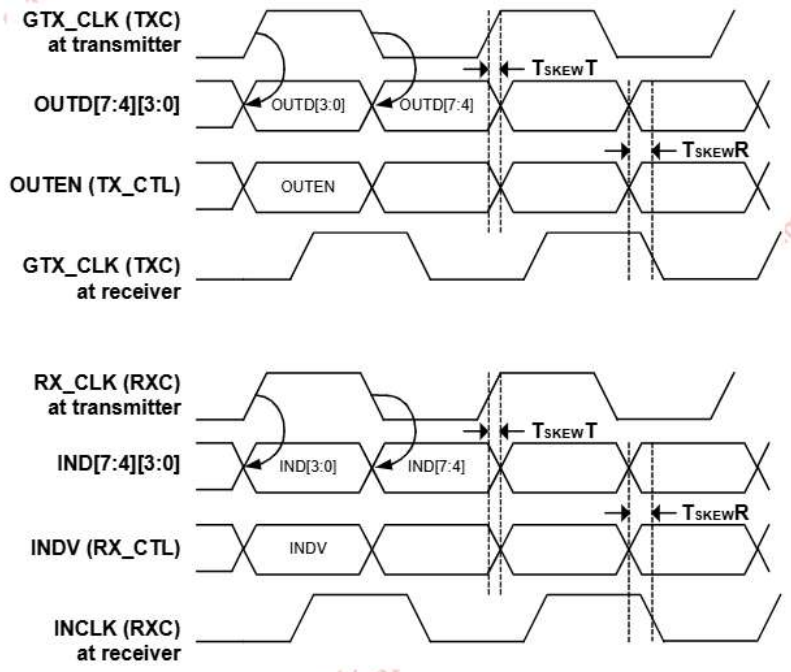
Table 37: RGMII Interface Timing

For other timing modes see Section 3.9.1, RGMII Timing for Different RGMII Modes, on page 80.

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.6	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T [1]	3.6	4.0	4.4	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20-80%)			0.75	ns

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three TCYCLE of the lowest speed transitioned between.

Figure 33: RGMII Multiplexing and Timing



3.9.1 RGMII Timing for Different RGMII Modes

3.9.1.1 RGMII Transmit Timing

Table 38: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{sskew}	RGMII Transmit Delay Control (bit 3) = 0	-0.5		0.5	ns

Figure 34: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 0

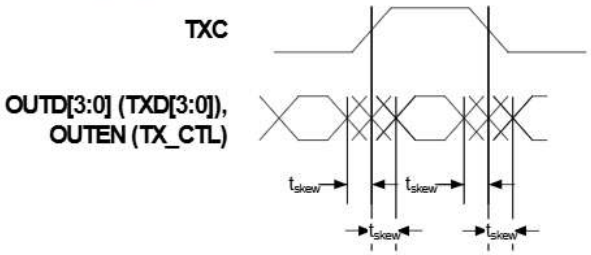
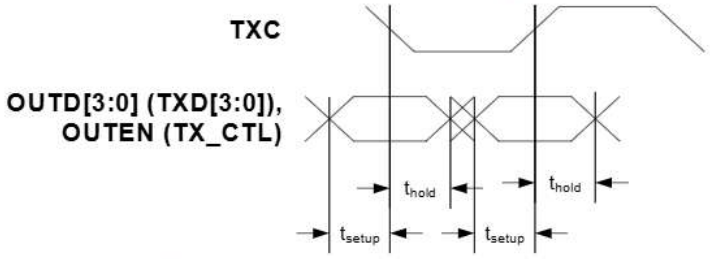


Table 39: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Transmit Delay Control (bit 3) = 1	1.2			ns
t_{hold}		1.2			ns

Figure 35: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 1



3.9.1.2 RGMII Receive Timing

Table 40: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 0	1.0			ns
t_{hold}		0.8			ns

Figure 36: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (bit 4) = 0

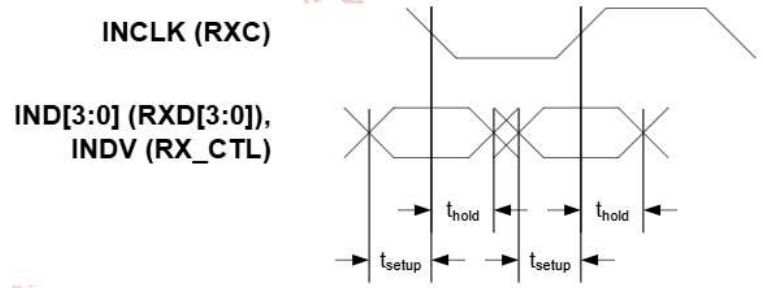
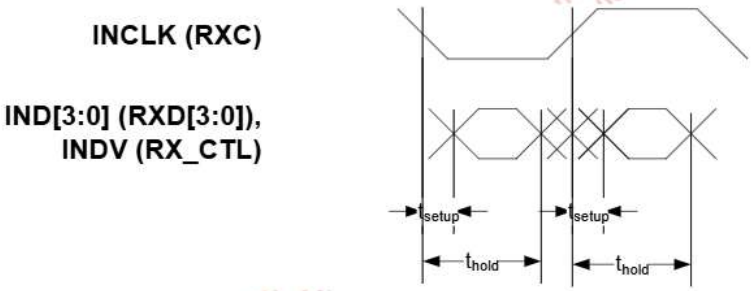


Table 41: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 1	-0.9			ns
t_{hold}		2.7			ns

Figure 37: Receive - RXC Timing when RGMII Receive Delay Control (bit 4) = 1



3.10 RMII Timing

3.10.1 RMII Receive Timing

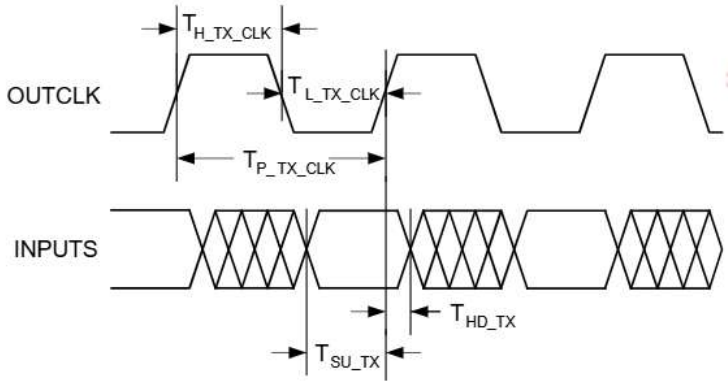
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 42: RMII Receive Timing using INCLK

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$	P[x]_OUTCLK period[1]	100BASE mode		20		ns
$T_{H\_TX\_CLK}$	P[x]_OUTCLK high	100BASE mode	8	10	12	ns
$T_{L\_TX\_CLK}$	P[x]_OUTCLK low	100BASE mode	8	10	12	ns
T_{SU_TX}	RMII inputs (P[x]_IND[1:0], P[x]_INDV) valid prior to P[x]_OUTCLK going high.		4			ns
T_{HD_TX}	RMII inputs (P[x]_IND[1:0], P[x]_INDV) valid after P[x]_OUTCLK going high.		2			ns

1. 50 MHz for 100 Mbps.

Figure 38: RMII Receive Timing using OUTCLK



NOTE: OUTCLK is the clock used to clock the input data. It is an output in this mode.

3.10.2 RMII Transmit Timing

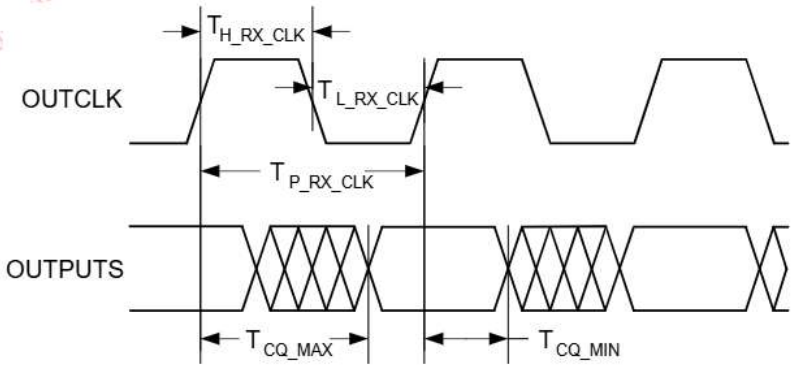
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 43: RMII Transmit Timing using INCLK

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	100BASE mode		20		ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	100BASE mode	8	10	12	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	100BASE mode	8	10	12	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[1:0], P[x]_OUTEN) valid				16	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[1:0], P[x]_OUTEN) invalid		2			ns

1. 50 MHz for 100 Mbps.

Figure 39: RMII Transmit Timing using OUTCLK



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

3.11 Serial Management Interface (SMI) Timing

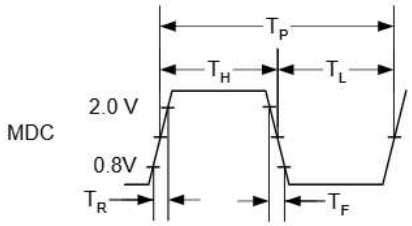
3.11.1 SMI Clock Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 44: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		50			ns	20 MHz
T_H	MDC high time		25			ns	
T_L	MDC low time		25			ns	
T_R	MDC rise				3	ns	
T_F	MDC fall				3	ns	

Figure 40: SMI Clock Timing (CPU Set)



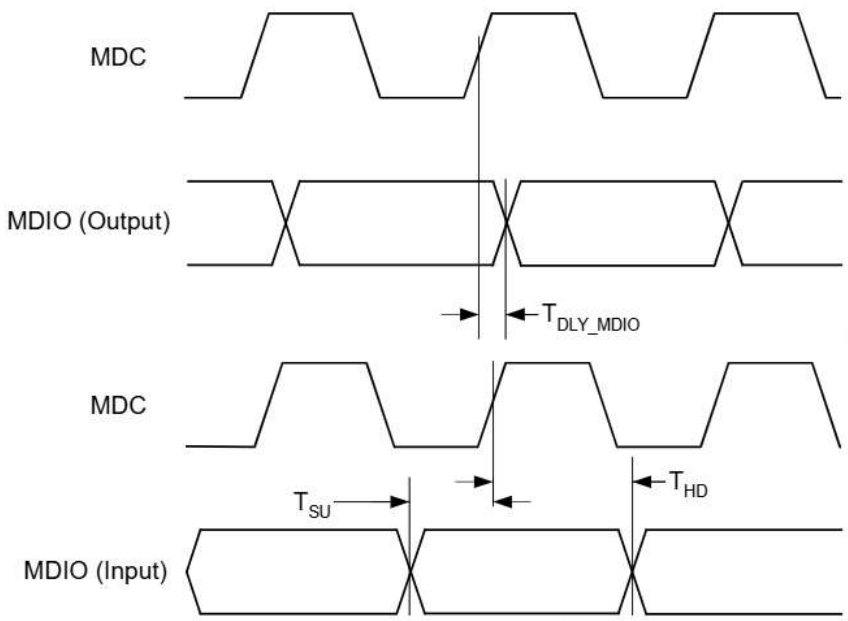
3.11.2 SMI Data Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 45: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		30	ns	
T_{SU}	MDIO (Input) to MDC setup time		10			ns	
T_{HD}	MDIO (Input) to MDC hold time		10			ns	

Figure 41: SMI Data Timing



3.11.3 SMI Timing (PHY Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 46: SMI Clock Timing (PHY Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		10			ns	9.09 MHz
T_H	MDC high time		48			ns	
T_L	MDC low time		48			ns	
T_R	MDC rise				6	ns	
T_F	MDC fall				6	ns	
T_{TX_SU}	MDIO output setup time		10			ns	1
T_{TX_HD}	MDIO output hold time		10			ns	2
T_{RX_SU}	MDIO input setup time						
T_{RX_HD}	MDIO input hold time						
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		5	ns	2

1. MDIO input setup and hold time is intentionally sampled with respect to the MDC falling edge.
2. MDIO data is intentionally clocked out on the falling edge of MDC.

Figure 42: SMI Timing Output (PHY Mode)

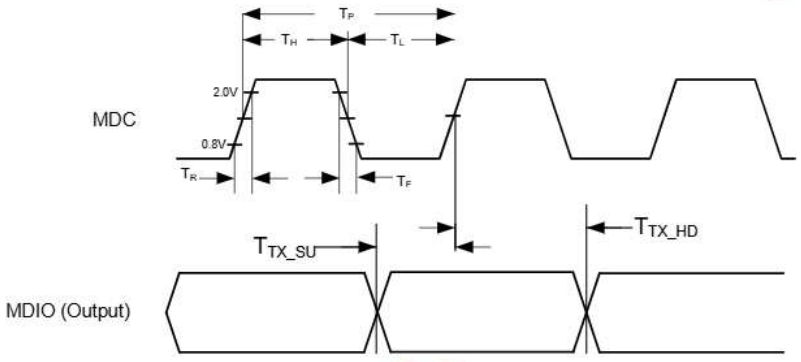
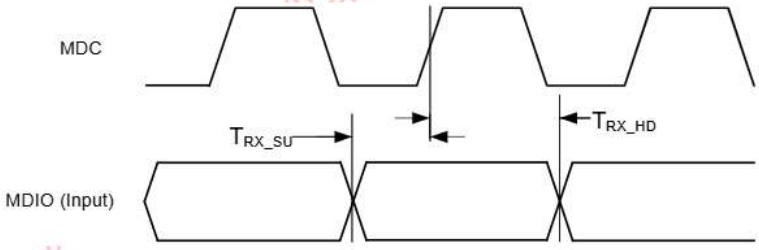


Figure 43: SMI Timing Input (PHY Mode)



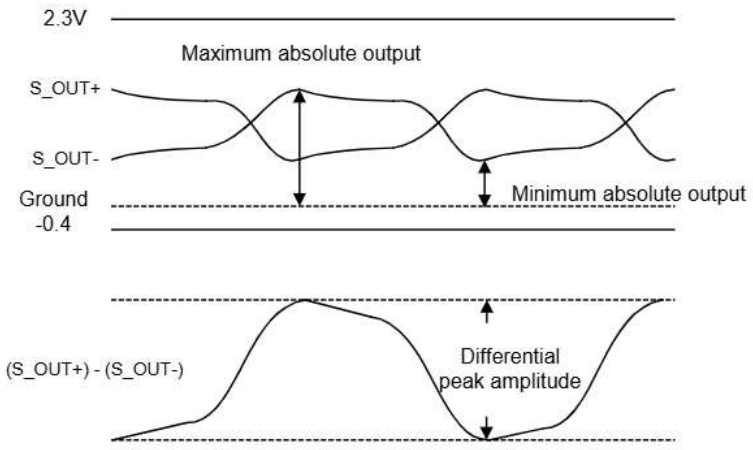
3.12 2500BASE-X

3.12.1 2500BASE-X Characteristics

Table 47: 2500BASE-X Characteristics

Symbol	Parameter	Min	Typ	Max	Units
	Baud rate		3.125		Gbd
	Unit interval		320		ps
	Differential amplitude	800		1600	mVp-p
Near-end Output Jitter					
	Deterministic Jitter			0.17	ui
	Total Jitter		0.2	0.35	ui
Far-end Output Jitter					
	Deterministic Jitter			0.37	ui
	Total Jitter			0.55	ui

Figure 44: Driver Output Voltage Limits and Definitions



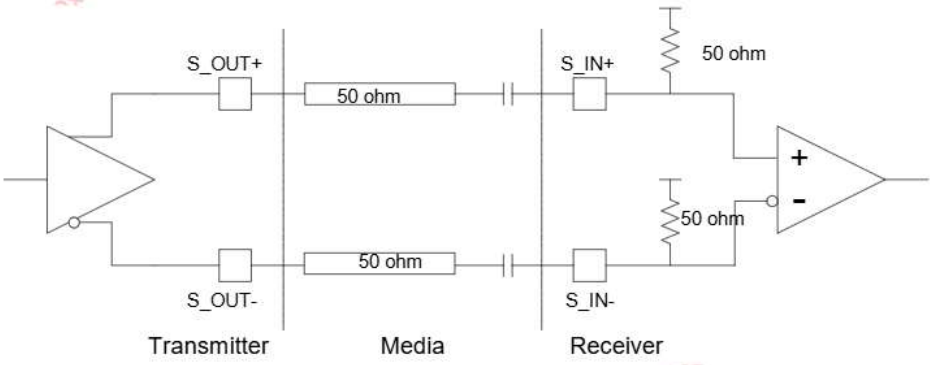
S_OUT+ and S_OUT- are the Positive and Negative Sides of the Differential Signal Pair for Lane i (i = 0, 1, 2, 3)

Table 48: Receiver Input Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Baud rate			3.125		Gbd
	Baud rate tolerance				±100	ppm
	Unit interval (UI)			320		ps
	Differential input amplitude[1]		200		1600	mVp-p
	Return loss[2]	Differential			10	dB
		Common mode			6	dB
	Jitter amplitude tolerance[3]	Peak-Peak total jitter			0.65	UIp-p
		Peak-Peak deterministic jitter			0.47	UIp-p

1. See 47.3.4.3 for detailed receive signal parameters in IEEE 802.3ae.
2. Measured from 100 MHz to 2.5 GHz. See clause 47.3.43 in IEEE 802.3ae for details.
3. See 47.3.4.6 for jitter tolerance details. The maximum random jitter is equal to the maximum total jitter minus the actual deterministic jitter.

Figure 45: High-Speed I/O AC Coupled Mode



The interface shall be AC coupled to allow for maximum inter-operability.

3.13 EEPROM Timing

3.13.1 2-Wire EEPROM Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 49: 2-Wire EEPROM Input Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
Freq	EE_CLK frequency	3.3V			1	Mhz
T_H	EE_CLK high time	3.3V	500			ns
T_L	EE_CLK low time	3.3V	500			ns
T_{IN}	Data input time	3.3V	50			ns

Figure 46: 2-Wire Input Timing

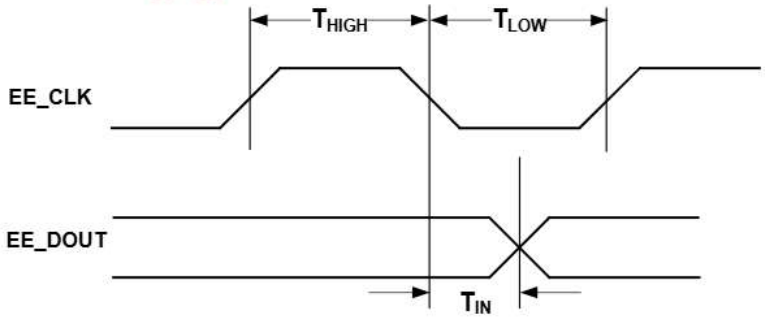
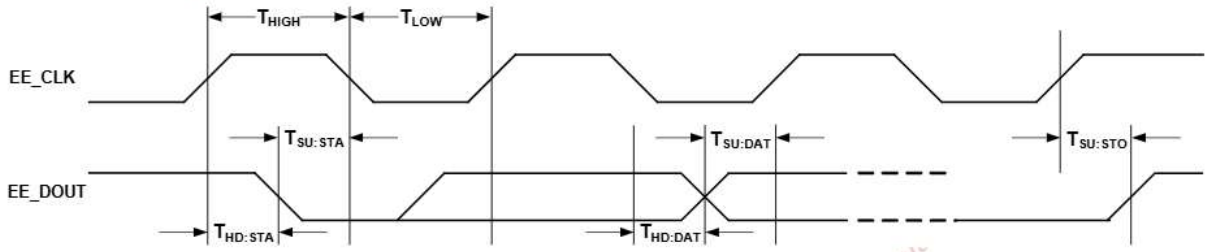


Table 50: 2-Wire EEPROM Output Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
Freq	EE_CLK frequency	3.3V			1000	kHz
T_H	EE_CLK high time	3.3V	500			ns
T_L	EE_CLK low time	3.3V	500			ns
$T_{HD:STA}$	Start condition hold time	3.3V	250			ns
$T_{SU:STA}$	Start condition setup time	3.3V	250			ns
$T_{HD:DAT}$	EE_DOUT data output hold time	3.3V	250			ns
$T_{SU:DAT}$	EE_DOUT data output setup time	3.3V	250			ns
$T_{SU:STO}$	Start condition setup time	3.3V	250			ns

Figure 47: 2-Wire EEPROM Output Timing



3.13.2 IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14-2000
-100BASE-TX ANSI X3.263-1995
-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

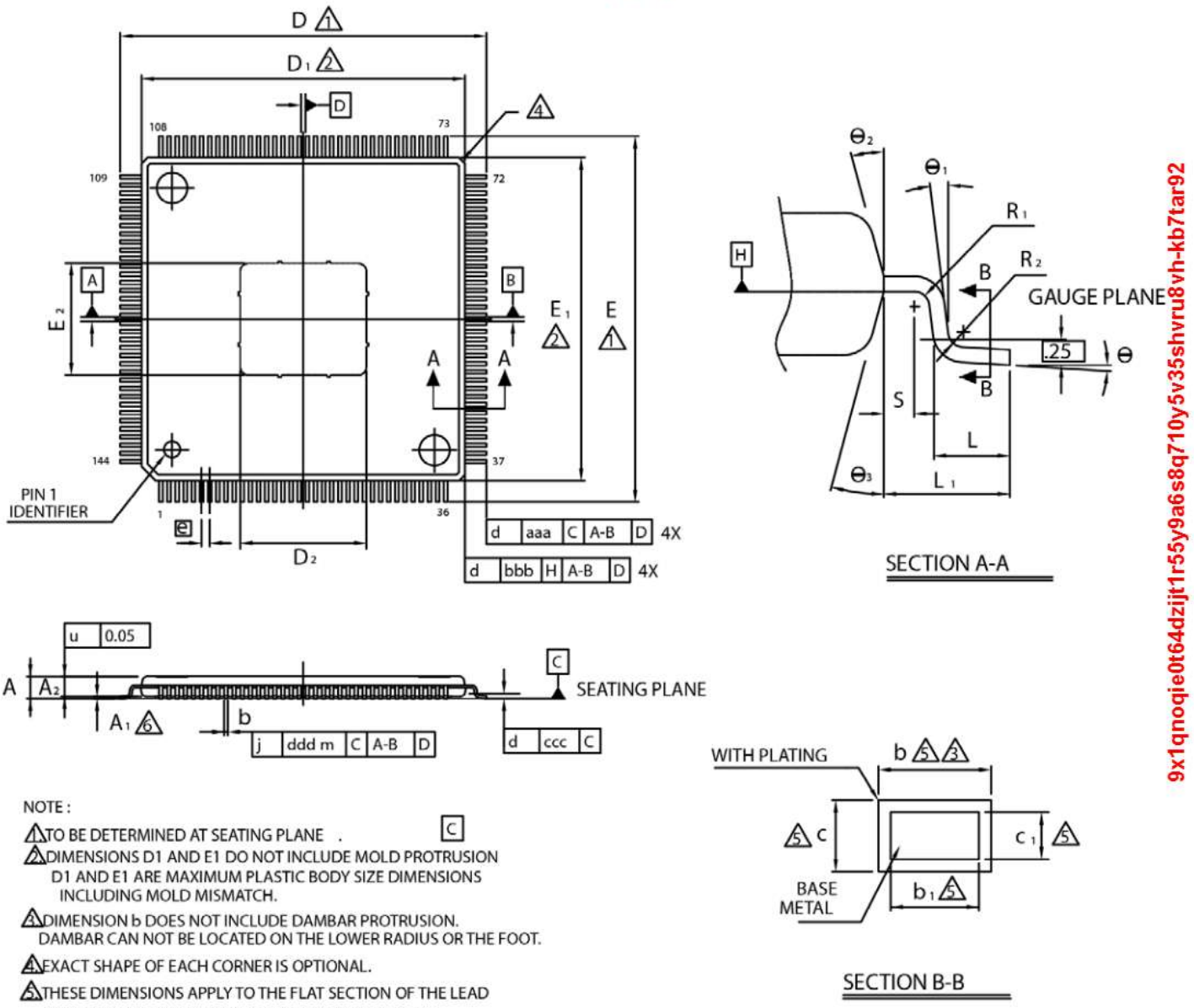
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall Time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{RISE}/ TFALL Symmetry		MDIP/N[1:0]	100BASE-TX	0		0.5	ns
DCD	Duty Cycle Distortion	MDIP/N[1:0]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		MDIP/N[1:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3

4 Mechanical Drawing

Figure 48: 144-pin E-PAD TQFP (16x16 mm) Mechanical Drawing



NOTE :

1. TO BE DETERMINED AT SEATING PLANE . C
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.

Table 51: 144-pin E-PAD TQFP (16x16 mm) Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	1.00	1.10	1.20
A_1	0.05	--	0.127
A_2	0.95	1.00	1.05
b	0.13	0.18	0.23
b_1	0.13	0.16	0.19
c	0.09	--	0.20
c_1	0.09	--	0.16
D		18.00 BSC	
D_1		16.00 BSC	
D_2	6.00 BSC	6.20 BSC	6.40 BSC
E		18.00 BSC	
E_1		16.00 BSC	
E_2	5.30 BSC	5.50 BSC	5.70 BSC
e		0.40 BSC	
L	0.45	0.60	0.75
L_1		1.00 REF	
R_1	0.08	--	--
R_2	0.08	--	0.20
S	0.20	--	--
θ	0°	3.5°	7°
θ_1	0°	--	--
θ_2	11°	12°	13°
θ_3	11°	12°	13°
aaa		0.20	
bbb		0.20	
ccc		0.08	
ddd		0.07	

5 Part Order Numbering/Package Marking

5.1 Part Order Numbering

Figure 49 shows the part order numbering scheme for the 88E6390/88E6190/88E6290. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 49: Sample Part Number

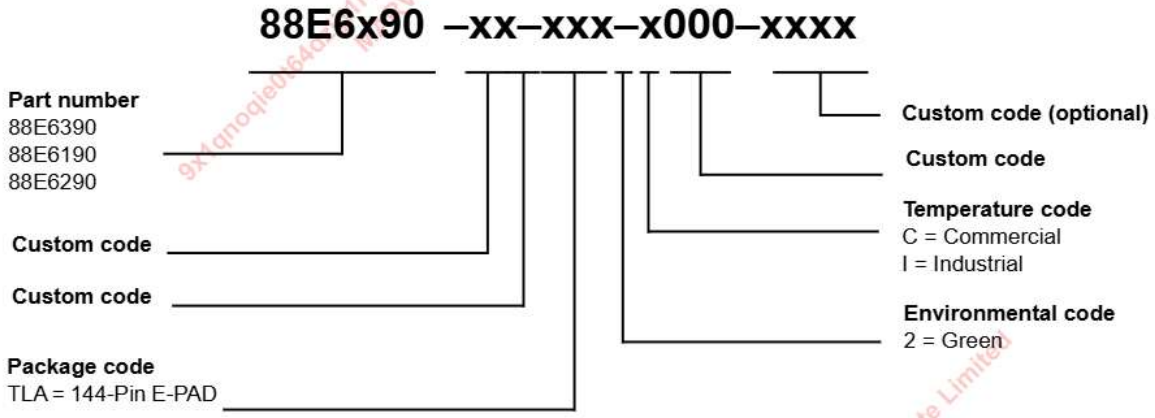


Table 52: 88E6390/88E6190/88E6290 Part Order Options

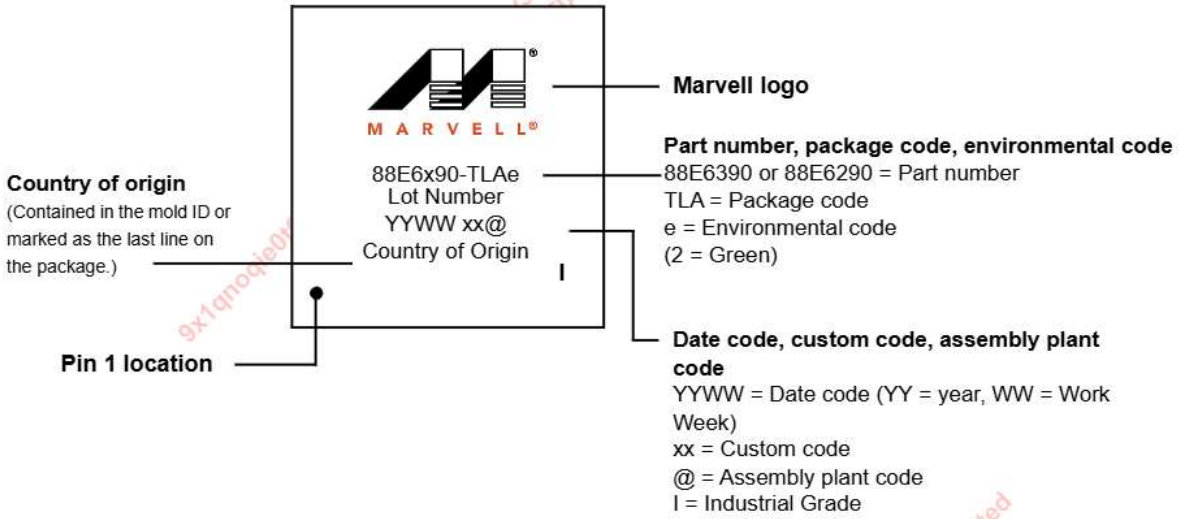
Package Type	Part Order Number
144-pin E-PAD TQFP (16x16 mm)	88E6390-xx-TLA2I000 (Industrial Green compliant package)
	88E6290-xx-TLA2I000 (Industrial Green compliant package)
	88E6390-xx-TLA2C000 (Commercial Green compliant package)
	88E6190-xx-TLA2C000 (Commercial Green compliant package)
	88E6290-xx-TLA2C000 (Commercial Green compliant package)

5.2 Package Marking

5.2.1 Industrial Package Marking

Figure 50 shows a sample Industrial package marking and pin 1 location for the 88E6390 and 88E6290 devices.

Figure 50: 88E6390 and 88E6290 Industrial Package Marking and Pin 1 Location

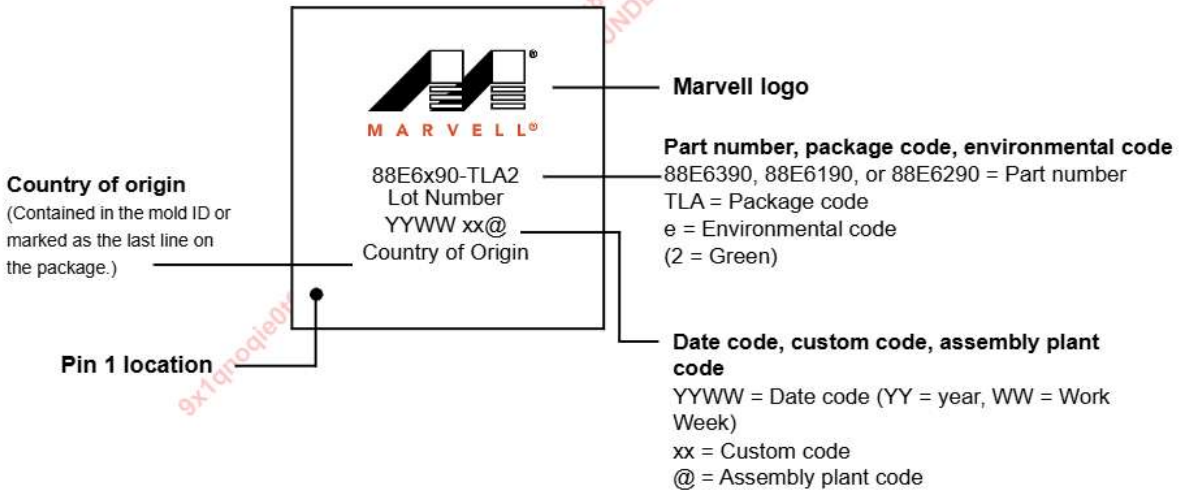


Note: The above drawing is not drawn to scale. Location of markings is approximate.

5.2.2 Commercial Package Marking

Figure 51 shows a sample Commercial package marking and pin 1 location for the 88E6390/88E6190/88E6290 devices.

Figure 51: Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

A Revision History

Table 53: Revision History (Sheet 1 of 3)

Revision	Date	Description
Rev. A v1.10	January 23, 2018	***Rev. A release.***
Rev. A v1.01	November 28, 2017	***Section 3, Electrical Specifications*** • Table 24, Digital Operating Conditions updated VDDO Parameter and Pins to separate EE_VDDO (3.3V) and P0_VDDO/GPIO_VDDO (2.5V/1.8V). Corrected V_{IL} All VDDO to EE_VDDO.
Rev. -- v1.00	September 7, 2017	***Initial release.***
Rev. -- v0.16	August 17, 2017	***Section 1, Signal Description*** • Table 9, System & Register Access, on page 31 MDC_CPU and MDIO_CPU pins - removed GPIO 3.3V tolerance in NOTE. • Table 10, Power & Ground, on page 32 P0_VDDO pin - removed "and the CPU interface" and GPIO 3.3V tolerance. • Table 10, Power & Ground, on page 32 GPIO_VDDO removed GPIO 3.3V tolerance. • Table 10, Power & Ground, on page 32 VDD_CORE updated definition to include I-temp ***Section 3, Electrical Specifications*** • Table 23, 88E6390/88E6190/88E6290 Device Current Consumption VDD_CORE to 1.1V • Table 24, Digital Operating Conditions V_{IH} All VDDO to EE_VDDO
Rev. -- v0.15	August 15, 2017	***Added Revision History*** ***Section 1, Signal Description*** • Table 6, Port 0 xMII Receive Interface, on page 25 updated Pin# 101, P0_CRS definition and updated table footnotes • Table 7, Port 0 xMII Transmit Interface, on page 28 updated table footnotes. • Table 9, System & Register Access, on page 31 Pin# 20 and 19, MDC_CPU and MDIO_CPU definitions - P0_VDDO to GPIO_VDDO • Table 10, Power & Ground, on page 32, Pin# 24, GPIO_VDDO added MDC_CPU and MDIO_CPU to definition. ***Section 2, Application Examples*** • Section 2.2.9, SERDES modes updated • Section 2.4, LED Interface updated • Figure 15, Typical SGMII connection to external PHY connections title updated ***Section 3, Electrical Specifications*** • Added Section 3.1.1, Power Supply Sequencing • Table 22, Recommended Operating Conditions updated • Table 23, 88E6390/88E6190/88E6290 Device Current Consumption added AVDD15_XTAL • Section 3.5.2, RESET, removed

Table 53: Revision History (Sheet 2 of 3)

Revision	Date	Description
Rev. -- v0.14	August 11, 2017	***Section 1, Signal Description*** • Table 6, Port 0 xMII Receive Interface, on page 25 updated Pin# 101, P0_CRS definition and updated table footnotes • Figure 8 through Figure 12 added resistors to figures
Rev. -- v0.13	December 15, 2016	***Section 1, Signal Description*** • Figure 4 and Figure 5 updated pin names to remove Px_LEDx names from pins 5, 6, 9, 10, 11, 12, 13 and 15 • Table 5, Port Status LEDs, on page 22 updated pin names to remove Px_LEDx names • Table 12, Pin List—Alphabetical by Signal Name, on page 34 updated pin names to remove Px_LEDx names from pins 5, 6, 9, 10, 11, 12, 13 and 15 ***Section 4, Mechanical Drawing*** • Table 51, 144-pin E-PAD TQFP (16x16 mm) Package Dimensions, on page 93 updated D2 and E2 dimensions
Rev. -- v0.12	December 14, 2016	***Section 2, Application Examples*** • Table 17, LED Mapping, on page 49 updated table column headings
Rev. -- v0.11	December 9, 2016	***Section 1, Signal Description*** • Table 10, Power & Ground, on page 32 VDD_CORE from 1.05V to 1.1V
Rev -- v0.10	November 9, 2016	Removed all edit marks.
Rev. -- v0.09	October 27, 2016	***Section 5, Part Order Numbering/Package Marking*** • Table 52, 88E6390/88E6190/88E6290 Part Order Options, on page 94 added 88E6290 I-Grade
Rev. -- v0.08	October 28, 2016	***Section , Overview*** • Table 1, 88E6390/88E6190/88E6290 Device Differences updated table • Figure 2, 88E6190 Block Diagram and Figure 3, 88E6290 Block Diagram, updated figures ***Section 1, Signal Description*** • Table 2, Network 1G/2.5G SERDES Interface (Ports 9 to 10) updated pin definitions • Table 4, Reference, Clock and Reset updated XTAL_IN, SE_SCLK and RESETn pin definitions • Table 5, Port Status LEDs updated Px_LED, EE_DOUT and C3_LED pin definitions • Table 6, Port 0 xMII Receive Interface updated P0_INCLK, P0_INDV, P0_CRS and P0_COL definitions • Table 7, Port 0 xMII Transmit Interface updated P0_OUTEN definition • Table 8, GPIO updated GPIO[x] and Px_SMODE definitions • Table 9, System & Register Access updated TEST definition • Table 10, Power & Ground updated P0_VDDO and GPIO_VDDO definitions ***Section 3, Electrical Specifications*** • Section Table 22:, Recommended Operating Conditions added I-grade details

Table 53: Revision History (Sheet 3 of 3)

Revision	Date	Description
Rev. -- v0.08 (cont.)	October 28, 2016	• Table 23, 88E6390/88E6190/88E6290 Device Current Consumption added Typ values • Table 46, SMI Clock Timing (PHY Set) updated MDC period values, removed footnote 1 • Table 49, 2-Wire EEPROM Input Timing updated Freq and T_{IN} values ***Section 5, Part Order Numbering/Package Marking*** • Added I-grade details
Rev. -- v0.07	October 26, 2016	***Section , Overview*** • Table 1, 88E6390/88E6190/88E6290 Device Differences updated table
Rev. -- v0.06	September 09, 2016	***Section , Overview*** • Started adding 88E6190 and 88E6290 device details throughout • Table 1, 88E6390/88E6190/88E6290 Device Differences added table • Figure 2, 88E6190 Block Diagram and Figure 3, 88E6290 Block Diagram, added figures ***Section 2, Application Examples*** added section ***Section 5, Part Order Numbering/Package Marking*** • Added 88E6190 and 88E6290 details
Rev. -- v0.05	September 29, 2015	***Section 1, Signal Description*** • Table 5, Port Status LEDs added PD resistors to EE_CLK, C2_LED and C3_LED Type • Table 6, Port 0 xMII Receive Interface Pin 100 renamed from P5_COL to P0_COL
Rev. -- v0.04	September 24, 2015	***Section 3, Electrical Specifications*** • Table 3.3.1, Thermal Conditions for the 88E6390/88E6190/88E6290 device 144-pin QFP Package added Typ values
Rev.-- v0.03 - v0.01	August 4, 2015 - September 21, 2015	***Created datasheet.***

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